

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
10	0001231154	ENGINEERING RELEASED		2011-09-06

J2 MLB - DVT OK2FAB

LAST_MODIFIED= Tue Sep 6 17:35:11 2011

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table of Contents	MIKE	NA
2	2	BLOCK DIAGRAM: SYSTEM	J2DEV	N/A
3	4	BOM TABLES	MIKE	N/A
4	6	AP: MAIN	MIKE	N/A
5	7	AP: I/Os	JOE	N/A
6	8	AP: NAND	MIKE	N/A
7	9	AP: TV, DP, MIPI	JOE	01/13/2011
8	10	AP: DDR	MIKE	N/A
9	11	AP: POWER	MIKE	N/A
10	12	AP: MISC & ALIASES	ALEX	N/A
11	13	AP: VIDEO BUFFER, BB USB MUXES	CHOPIN	12/10/2010
12	14	NAND	MIKE	N/A
13	16	DDR 0 AND 1	MIKE	06/21/2010
14	17	DDR 2 AND 3	MIKE	06/21/2010
15	21	MLB ALIASES/CONNECTIONS	ALEX	09/30/2010
16	22	VIDEO: EDP CONNECTOR	JOE	01/19/2011
17	30	GRAPE: GROUNDHOG, CONN, BOOST	RAMSIN	12/17/2010
18	31	GRAPE: Z1, Z2	RAMSIN	12/17/2010
19	36	AUDIO: L63B CODEC	KAVITHA	02/03/2011
20	37	AUDIO: SPEAKER AMP	KAVITHA	02/03/2011
21	38	AUDIO: HEADPHONE OUT	KAVITHA	02/03/2011
22	42	AUDIO: DETECT/MIC BIAS	KAVITHA	02/03/2011
23	43	AUDIO: HP/MIC FILTERS	KAVITHA	02/03/2011
24	54	CONNECTOR: SENSOR	MARK	01/11/2011
25	55	SENSOR PANEL FILTERS 1	MARK	01/11/2011
26	56	SENSOR PANEL FILTERS 2	MARK	01/11/2011
27	57	IO FLEX: DOCK COMPONENTS	JOE	01/19/2011
28	58	DISPLAY PORT MISC	JOE	01/19/2011
29	59	IO FLEX: B2B CONNECTOR	JOE	01/19/2011
30	60	CONNECTOR: X26	JOE	01/19/2011
31	61	WLAN BB & POWER	X26_WIFI_MIKE_BT	09/01/2011

PDF	CSA	CONTENTS	SYNC MASTER	DATE
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33	63	WLAN 5GHZ AND TEST POINTS	X26_WIFI_MIKE_BT	09/01/2011
34	75	POWER: BATTERY CONNECTOR	MADHAVI	01/13/2011
35	80	POWER ALIASES	MADHAVI	01/13/2011
36	81	POWER: AMELIA PMU	MADHAVI	01/13/2011
37	82	POWER: AMELIA PMU	MLB	01/14/2011
38	83	POWER: AMELIA VSS	MADHAVI	01/13/2011
39	90	DEBUG AND MISC	ALEX	10/04/2010
40	93	FCT/ICT TEST/BRACKETS	ALEX	10/04/2010
41	150	CONSTRAINTS: MLB RULES	MIKE	01/21/2011
42	151	CONSTRAINTS: LOW SPEED BUS	MIKE	01/21/2011
43	152	CONSTRAINTS: DISPLAY/AUDIO	MIKE	01/21/2011
44	153	CONSTRAINTS: DDR/FMI	MIKE	01/21/2011
45	154	CONSTRAINTS: POWER / GND	MIKE	01/21/2011
46	155	CONSTRAINTS: DEBUG	MIKE	01/21/2011
47	156	FUNC TEST POINTS	MIKE	01/21/2011
48	157	FUNC TEST POINTS	MIKE	01/21/2011

DRAWING
 DRAWING
 MLB
 Schematic / PCB #'s

DRAWING TITLE		SCH, J2, MLB	
DRAWING NUMBER		051-8773	SIZE D
REVISION		10.0.0	
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD
128GB_PROD

DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_DAP

SPEAKER
INTERNAL_MIC

NAND_IO LV8
NAND_IO=3V3

SNOTE
DEV
MLB
JZ

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE
AUDIO	SPEAKER, INTERNAL_MIC

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-2352 (J1 16G)	EEEE_DNKT	CRITICAL	EEEE_J1_16G
825-7691	1	EEEE FOR 639-2058 (J1 32G)	EEEE_DM2N	CRITICAL	EEEE_J1_32G
825-7691	1	EEEE FOR 639-2059 (J1 64G)	EEEE_DM2P	CRITICAL	EEEE_J1_64G
825-7691	1	EEEE FOR 639-2353 (J2 16G)	EEEE_DNKV	CRITICAL	EEEE_J2_16G
825-7691	1	EEEE FOR 639-1572 (J2 32G)	EEEE_DHWV	CRITICAL	EEEE_J2_32G
825-7691	1	EEEE FOR 639-1871 (J2 64G)	EEEE_DKQL	CRITICAL	EEEE_J2_64G
825-7691	1	EEEE FOR 639-1870 (J2 128G)	EEEE_DKQK	CRITICAL	EEEE_J2_128G
825-7691	1	EEEE FOR 639-2844 (J2A 16G)	EEEE_DRJQ	CRITICAL	EEEE_J2A_16G
825-7691	1	EEEE FOR 639-2826 (J2A 32G)	EEEE_DRP6	CRITICAL	EEEE_J2A_32G
825-7691	1	EEEE FOR 639-2827 (J2A 64G)	EEEE_DRP5	CRITICAL	EEEE_J2A_64G

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-2105	1	FENCE, NAND, TOP, MLB, J2	PD_FENCE_NAND	CRITICAL	
806-1857	1	FENCE, LARGE, TOP, MLB, J2	PD_FENCE_LARGE	CRITICAL	
806-2349	1	FENCE, SMALLER, TOP, MLB, J2	PD_FENCE_SMALL	CRITICAL	
806-1860	1	FENCE, 1, BTM, MLB, J2	PD_FENCE_BTM1	CRITICAL	
806-1865	1	FENCE, 2, BTM, MLB, J2	PD_FENCE_BTM2	CRITICAL	
806-2352	1	FENCE, SMALLER, BTM, MLB, J2	PD_FENCE_BTM3	CRITICAL	

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8773	1	SCH, MLB, J2	SCH1	CRITICAL	?
820-2996	1	PCBF, MLB, J2	PCB1	CRITICAL	?
085-3058	1	DEV BOM, MLB, J2	DEV1		?

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380533	1	IC, SOC, H4G, FCBGA1225	U0600	CRITICAL	?

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380561	1	IC, PMU, AMELIA, D1974AB	U8100	CRITICAL	?

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33380579	2	SDRAM, LPDDR2, 512MB, SAMSUNG 46NM	U1600, U1700	CRITICAL	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33380580	33380579		U1600, U1700	LPDDR2, HYNIX 44NM
33380581	33380579		U1600, U1700	LPDDR2, ELPIDA 45NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33580781	1	HYNIX 26NM PPN1.0 16GB	U1400	CRITICAL	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580804	33580781	16GB_PROD	U1400	TOSHIBA 24NM PPN1.0

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33580781	2	HYNIX 26NM PPN1.0 32GB	U1400, U1410	CRITICAL	32GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580804	33580781	32GB_PROD	U1400, U1410	TOSHIBA 24NM PPN1.0

64GB FLASH CONFIGURATIONS


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33580782	2	HYNIX 26NM PPN1.0 64GB	U1400, U1410	CRITICAL	64GB_PROD

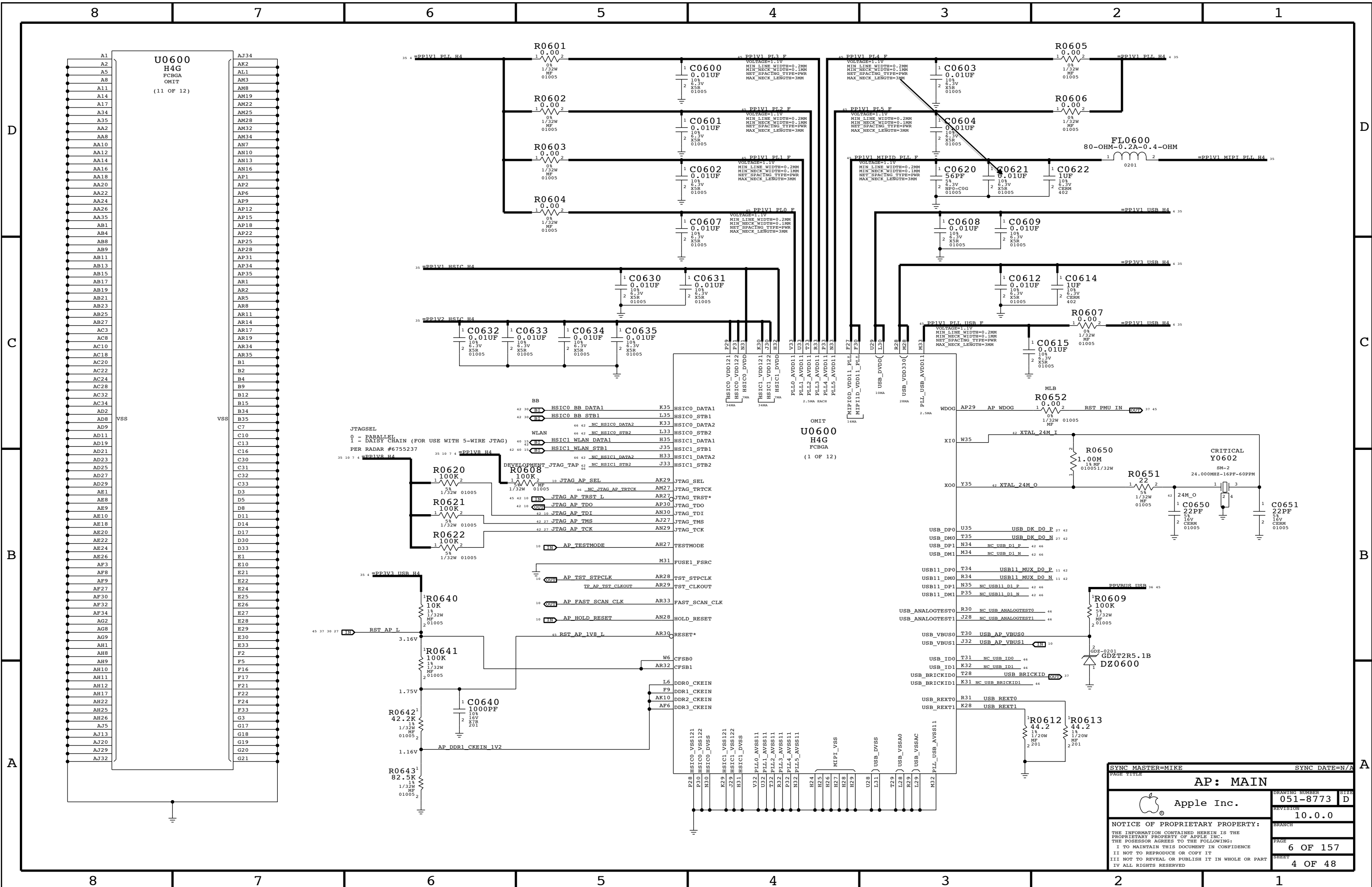
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580805	33580782	64GB_PROD	U1400, U1410	TOSHIBA 24NM PPN1.0

128GB FLASH CONFIGURATIONS

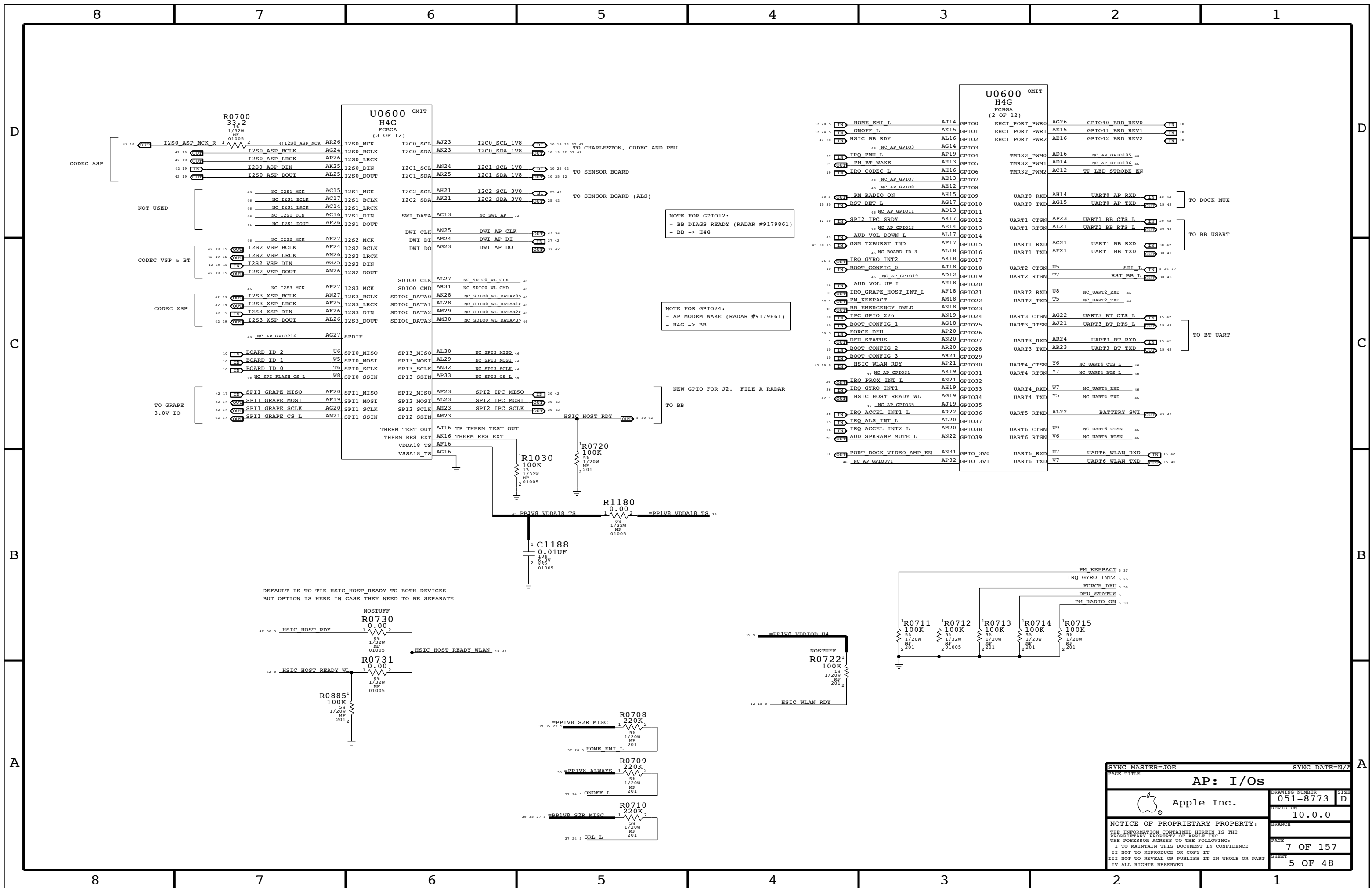
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33580814	2	HYNIX 26NM PPN1.0 64GB	U1400, U1410	CRITICAL	128GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580806	33580814	128GB_PROD	U1400, U1410	TOSHIBA 24NM PPN1.0

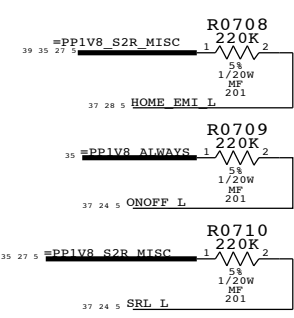
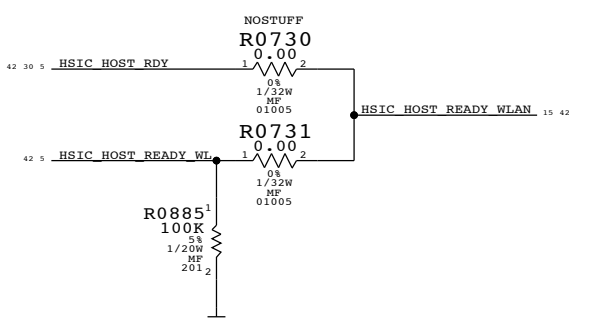
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DEFAULT IS TO TIE HSIC_HOST_READY TO BOTH DEVICES
BUT OPTION IS HERE IN CASE THEY NEED TO BE SEPARATE



NOTE FOR GPIO12:
- BB_DIAGS_READY (RADAR #9179861)
- BB -> H4G

NOTE FOR GPIO24:
- AP_MODEM_WAKE (RADAR #9179861)
- H4G -> BB

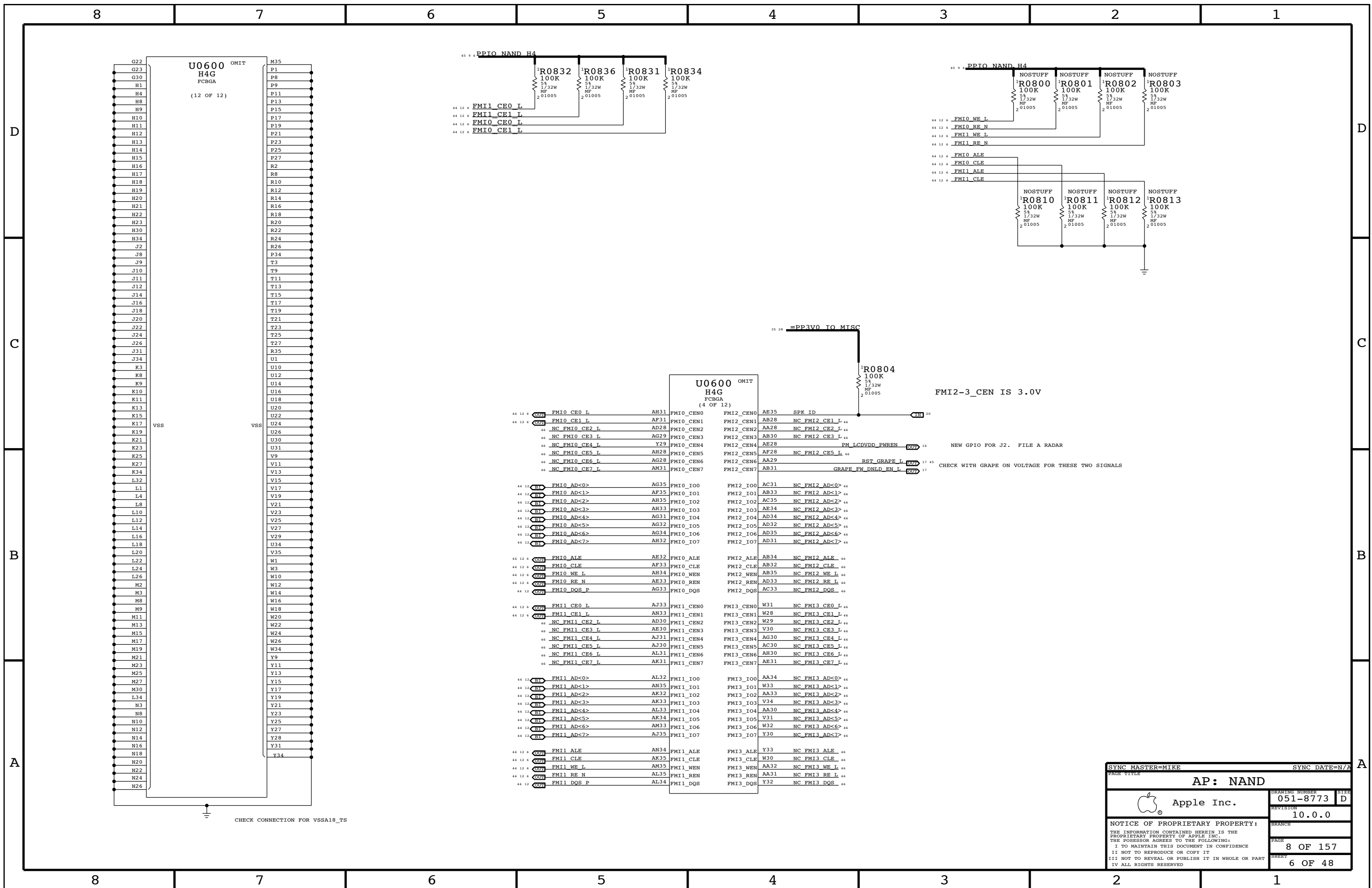
NEW GPIO FOR J2. FILE A RADAR
TO BB

U0600 OMIT
H4G
FCBGA
(2 OF 12)

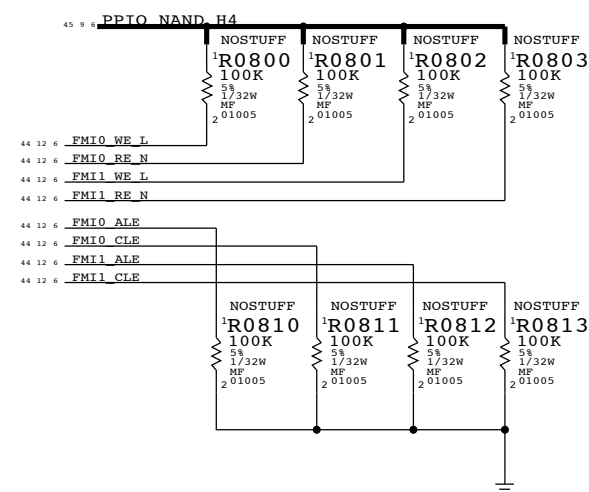
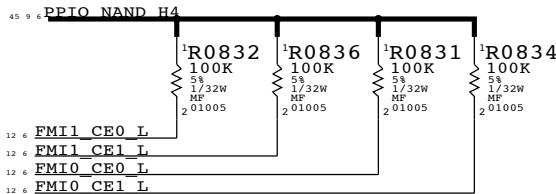
37 28 5	HOME_EMI_L	AJ14	GPIO0
37 24 5	ONOFF_L	AK15	GPIO1
42 30	HSIC_BB_RDY	AL16	GPIO2
	NC AP GPIO3	AG14	GPIO3
37	IRO_PMU_L	AP19	GPIO4
15	PM_BT_WAKE	AH13	GPIO5
19	IRO_CODEC_L	AH16	GPIO6
	NC AP GPIO7	AE13	GPIO7
	NC AP GPIO8	AE12	GPIO8
30 5	PM_RADIO_ON	AH15	GPIO9
45 30	RST_DET_L	AG17	GPIO10
	NC AP GPIO11	AD13	GPIO11
42 30	SPI2_IPC_SRDY	AK17	GPIO12
	NC AP GPIO13	AE14	GPIO13
24	AUD_VOL_DOWN_L	AL17	GPIO14
45 30 15	GSM_TXBURST_IND	AF17	GPIO15
	NC_BOARD_ID_3	AK18	GPIO16
26 5	IRO_GYRO_INT2	AK18	GPIO17
10	BOOT_CONFIG_0	AJ18	GPIO18
	NC AP GPIO19	AD12	GPIO19
24	AUD_VOL_UP_L	AH18	GPIO20
	IRO_GRAPE_HOST_INT_L	AF18	GPIO21
37 5	PM_KEEPACT	AM18	GPIO22
30	BB_EMERGENCY_DWLD	AN18	GPIO23
	IPC_GPIO_X26	AN19	GPIO24
10	BOOT_CONFIG_1	AG18	GPIO25
	FORCE_DFU	AP20	GPIO26
39 5	DFU_STATUS	AN20	GPIO27
10	BOOT_CONFIG_2	AR20	GPIO28
	BOOT_CONFIG_3	AR21	GPIO29
10	HSIC_WLAN_RDY	AP21	GPIO30
42 15 5	NC AP GPIO31	AK19	GPIO31
26	IRO_PROX_INT_L	AN21	GPIO32
	IRO_GYRO_INT1	AH19	GPIO33
42 5	HSIC_HOST_READY_WL	AG19	GPIO34
	NC AP GPIO35	AJ19	GPIO35
26	IRO_ACCEL_INT1_L	AR22	GPIO36
	IRO_ALS_INT_L	AL20	GPIO37
24	IRO_ACCEL_INT2_L	AM20	GPIO38
20	AUD_SPKRAMP_MUTE_L	AN22	GPIO39
11	PORT_DOCK_VIDEO_AMP_EN	AN31	GPIO_3V0
	NC AP GPIO3V1	AP32	GPIO_3V1

AG26	GPIO40_BRD_REV0	31N	10
AE15	GPIO41_BRD_REV1	31N	10
AE16	GPIO42_BRD_REV2	31N	10
AD16	NC AP GPIO185_46		
AD14	NC AP GPIO186_46		
AC12	TP_LED_STROBE_EN		
AH14	UART0_AP_RXD	31N	15 42
AG15	UART0_AP_TXD	31N	15 42
AP23	UART1_BB_CTS_L	31N	30 42
AL21	UART1_BB_RTS_L	31N	30 42
AG21	UART1_BB_RXD	31N	30 42
AF21	UART1_BB_TXD	31N	30 42
U5	SRL_L	31N	5 24 37
T7	RST_BB_L	31N	30 45
U8	NC UART2_RXD_46		
T5	NC UART2_TXD_46		
AG22	UART3_BT_CTS_L	31N	15 42
AJ21	UART3_BT_RTS_L	31N	15 42
AR24	UART3_BT_RXD	31N	15 42
AR23	UART3_BT_TXD	31N	15 42
Y6	NC UART4_CTS_L_46		
Y7	NC UART4_RTS_L_46		
W7	NC UART4_RXD_46		
Y5	NC UART4_TXD_46		
AL22	BATTERY_SWI	31N	34 37
U9	NC UART6_CTSN_46		
V6	NC UART6_RTSN_46		
U7	UART6_WLAN_RXD	31N	15 42
V7	UART6_WLAN_TXD	31N	15 42

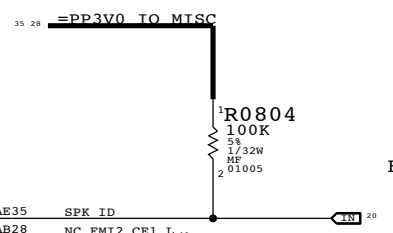
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H4G
FCBGA
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U0600 OMIT
H4G
FCBGA
(4 OF 12)



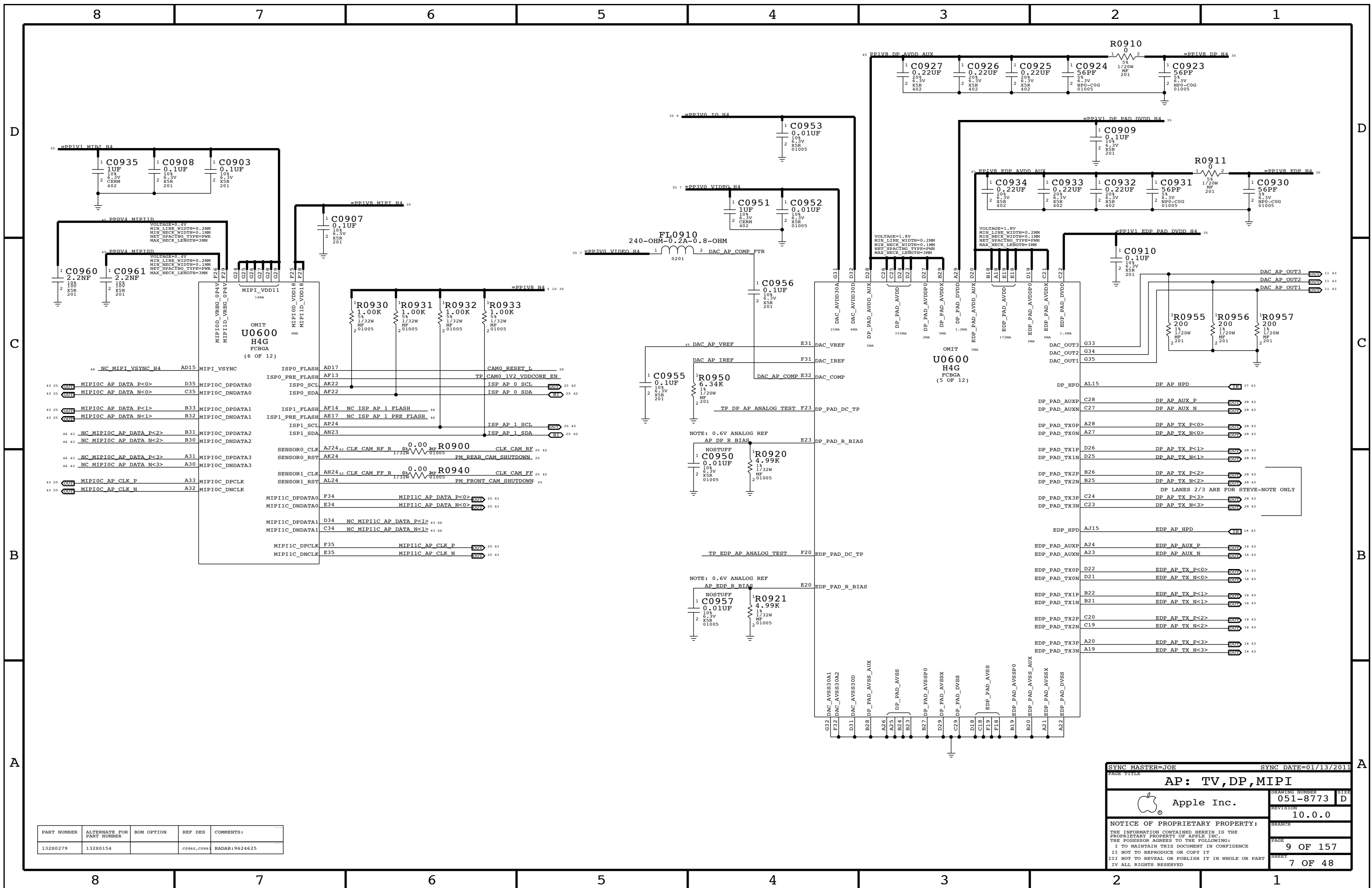
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44 12 6	OMIT	FMI0_CEI_L	AF31	FMI0_CEN1	FMI2_CEN1	AB28	NC FMI2_CEI_L	44
44	OMIT	NC FMI0_CE2_L	AD28	FMI0_CEN2	FMI2_CEN2	AA28	NC FMI2_CE2_L	44
44	OMIT	NC FMI0_CE3_L	AG29	FMI0_CEN3	FMI2_CEN3	AB30	NC FMI2_CE3_L	44
44	OMIT	NC FMI0_CE4_L	Y29	FMI0_CEN4	FMI2_CEN4	AE28	PM_LCDVDD_PWREN	16
44	OMIT	NC FMI0_CE5_L	AH28	FMI0_CEN5	FMI2_CEN5	AF28	NC FMI2_CE5_L	44
44	OMIT	NC FMI0_CE6_L	AG28	FMI0_CEN6	FMI2_CEN6	AA29	RST_GRAPE_L	17 45
44	OMIT	NC FMI0_CE7_L	AM31	FMI0_CEN7	FMI2_CEN7	AB31	GRAPE_FW_DNLD_EN_L	17
44 12	BE	FMI0_AD<0>	AG35	FMI0_IO0	FMI2_IO0	AC31	NC FMI2_AD<0>	44
44 12	BE	FMI0_AD<1>	AF35	FMI0_IO1	FMI2_IO1	AB33	NC FMI2_AD<1>	44
44 12	BE	FMI0_AD<2>	AH35	FMI0_IO2	FMI2_IO2	AC35	NC FMI2_AD<2>	44
44 12	BE	FMI0_AD<3>	AH33	FMI0_IO3	FMI2_IO3	AE34	NC FMI2_AD<3>	44
44 12	BE	FMI0_AD<4>	AG31	FMI0_IO4	FMI2_IO4	AD34	NC FMI2_AD<4>	44
44 12	BE	FMI0_AD<5>	AG32	FMI0_IO5	FMI2_IO5	AD32	NC FMI2_AD<5>	44
44 12	BE	FMI0_AD<6>	AG34	FMI0_IO6	FMI2_IO6	AD35	NC FMI2_AD<6>	44
44 12	BE	FMI0_AD<7>	AH32	FMI0_IO7	FMI2_IO7	AD31	NC FMI2_AD<7>	44
44 12 6	OMIT	FMI0_ALE	AE32	FMI0_ALE	FMI2_ALE	AB34	NC FMI2_ALE	44
44 12 6	OMIT	FMI0_CLE	AF33	FMI0_CLE	FMI2_CLE	AB32	NC FMI2_CLE	44
44 12 6	OMIT	FMI0_WE_L	AH34	FMI0_WEN	FMI2_WEN	AB35	NC FMI2_WE_L	44
44 12 6	OMIT	FMI0_RE_N	AE33	FMI0_REN	FMI2_REN	AD33	NC FMI2_RE_L	44
44 12	OMIT	FMI0_DQS_P	AG33	FMI0_DQS	FMI2_DQS	AC33	NC FMI2_DQS	44
44 12 6	OMIT	FMI1_CEO_L	AJ33	FMI1_CEN0	FMI3_CEN0	W31	NC FMI3_CEO_L	44
44 12 6	OMIT	FMI1_CEI_L	AN33	FMI1_CEN1	FMI3_CEN1	W28	NC FMI3_CEI_L	44
44	OMIT	NC FMI1_CE2_L	AD30	FMI1_CEN2	FMI3_CEN2	W29	NC FMI3_CE2_L	44
44	OMIT	NC FMI1_CE3_L	AE30	FMI1_CEN3	FMI3_CEN3	V30	NC FMI3_CE3_L	44
44	OMIT	NC FMI1_CE4_L	AJ31	FMI1_CEN4	FMI3_CEN4	AG30	NC FMI3_CE4_L	44
44	OMIT	NC FMI1_CE5_L	AJ30	FMI1_CEN5	FMI3_CEN5	AC30	NC FMI3_CE5_L	44
44	OMIT	NC FMI1_CE6_L	AL31	FMI1_CEN6	FMI3_CEN6	AH30	NC FMI3_CE6_L	44
44	OMIT	NC FMI1_CE7_L	AK31	FMI1_CEN7	FMI3_CEN7	AE31	NC FMI3_CE7_L	44
44 12	BE	FMI1_AD<0>	AL32	FMI1_IO0	FMI3_IO0	AA34	NC FMI3_AD<0>	44
44 12	BE	FMI1_AD<1>	AN35	FMI1_IO1	FMI3_IO1	W33	NC FMI3_AD<1>	44
44 12	BE	FMI1_AD<2>	AK32	FMI1_IO2	FMI3_IO2	AA33	NC FMI3_AD<2>	44
44 12	BE	FMI1_AD<3>	AK33	FMI1_IO3	FMI3_IO3	V34	NC FMI3_AD<3>	44
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44 12	BE	FMI1_AD<6>	AM33	FMI1_IO6	FMI3_IO6	W32	NC FMI3_AD<6>	44
44 12	BE	FMI1_AD<7>	AJ35	FMI1_IO7	FMI3_IO7	Y30	NC FMI3_AD<7>	44
44 12 6	OMIT	FMI1_ALE	AN34	FMI1_ALE	FMI3_ALE	Y33	NC FMI3_ALE	44
44 12 6	OMIT	FMI1_CLE	AK35	FMI1_CLE	FMI3_CLE	W30	NC FMI3_CLE	44
44 12 6	OMIT	FMI1_WE_L	AM35	FMI1_WEN	FMI3_WEN	AA32	NC FMI3_WE_L	44
44 12 6	OMIT	FMI1_RE_N	AL35	FMI1_REN	FMI3_REN	AA31	NC FMI3_RE_L	44
44 12	OMIT	FMI1_DQS_P	AL34	FMI1_DQS	FMI3_DQS	Y32	NC FMI3_DQS	44

NEW GPIO FOR J2. FILE A RADAR

CHECK WITH GRAPE ON VOLTAGE FOR THESE TWO SIGNALS

CHECK CONNECTION FOR VSSA18_T5

SYNC MASTER=MIKE		SYNC DATE=N/A	
AP: NAND			
Apple Inc.		DRAWING NUMBER	SIZE
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PAGE		8 OF 157	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
13280279	13280154		C0960, C0961	RADAR:9624625

SYNC MASTER=JOE SYNC DATE=01/13/2011

AP: TV, DP, MIPI

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

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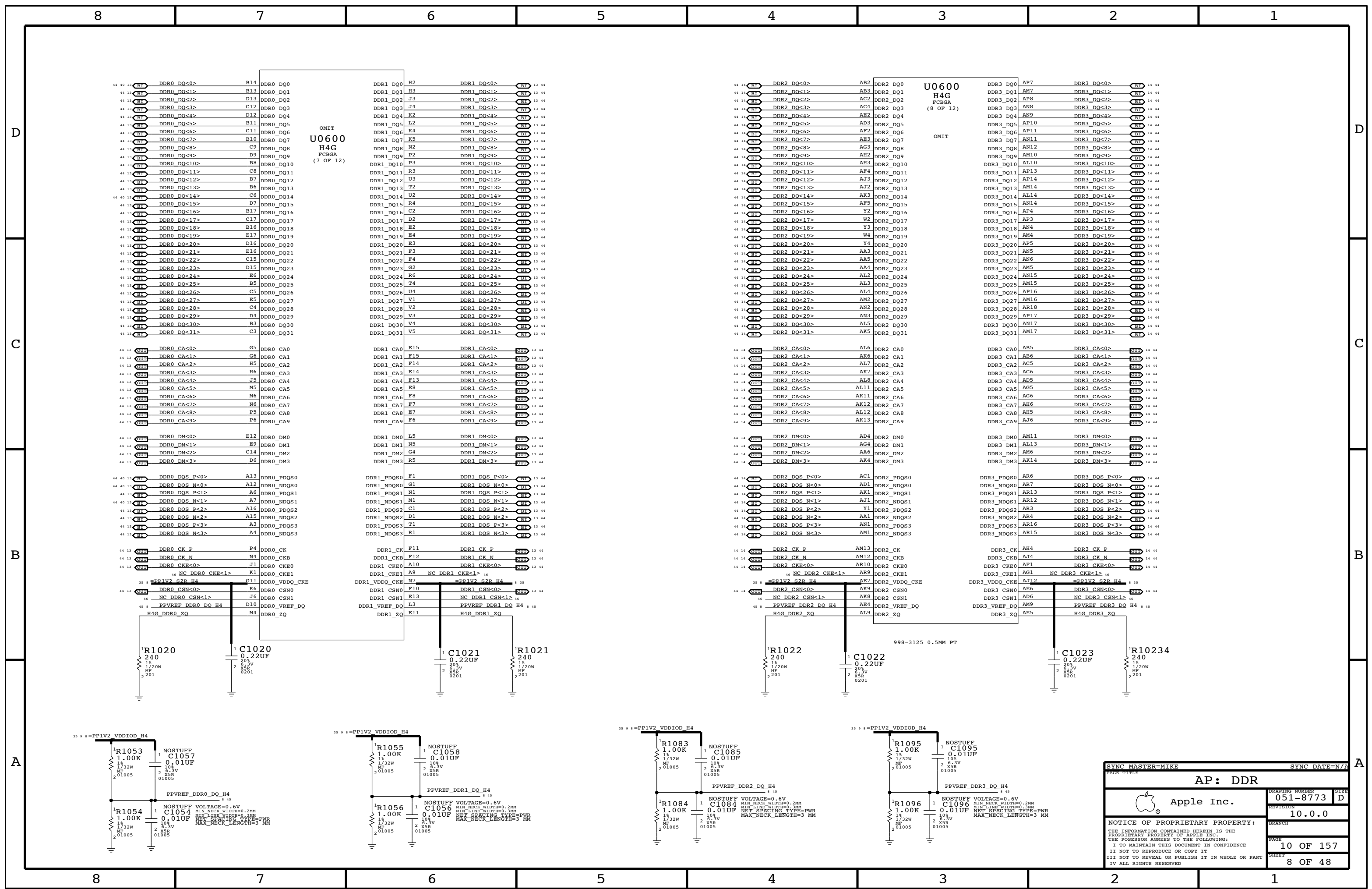
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PAGE: 9 OF 157

SHEET: 7 OF 48



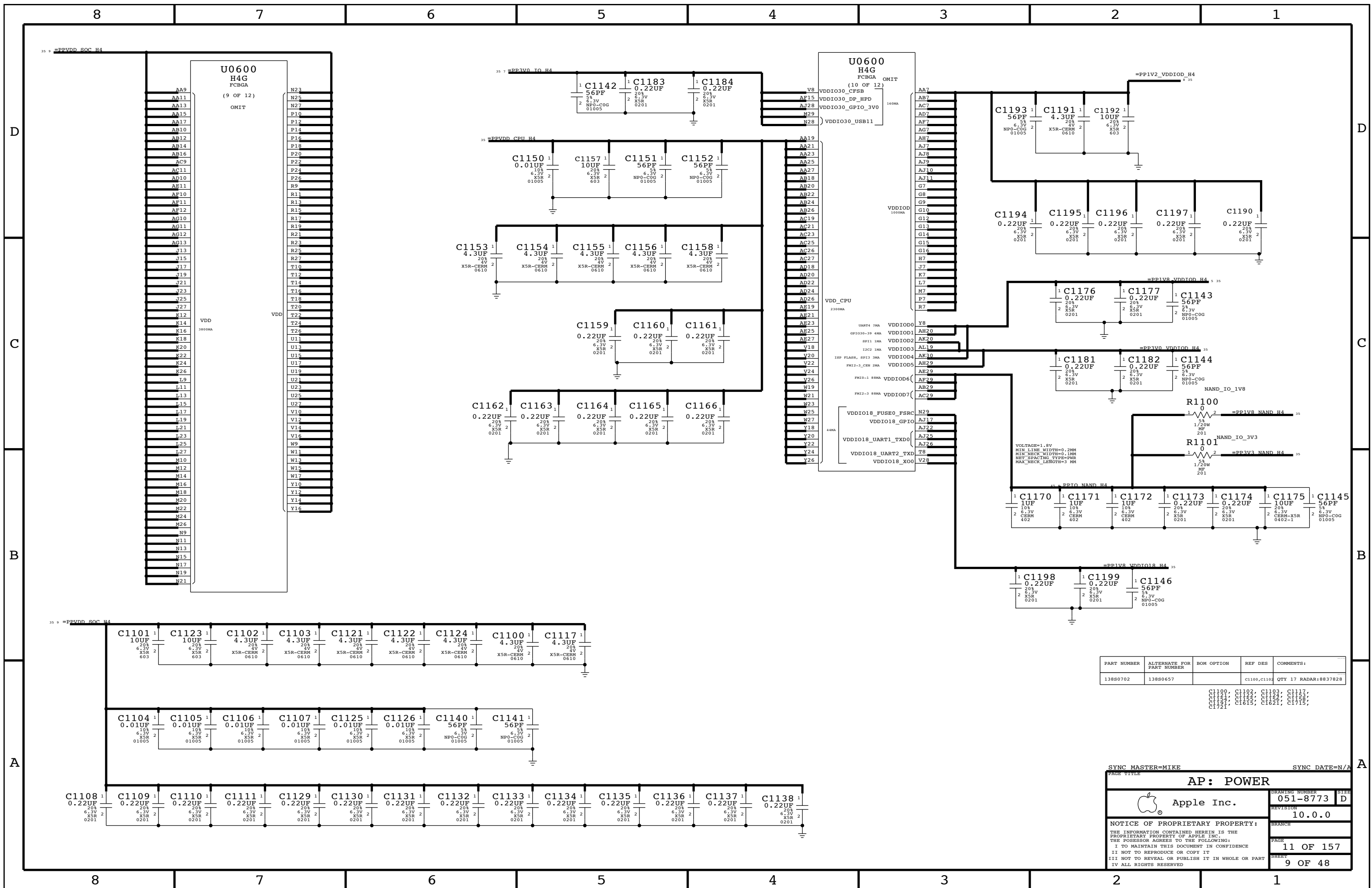
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U0600
H4G
FCBGA
(7 OF 12)

U0600
H4G
FCBGA
(8 OF 12)

OMIT

PAGE TITLE		SYNC DATE=N/A	
AP: DDR			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8773	D
		REVISION	
		10.0.0	
		BRANCH	
		PAGE	
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		SHEET	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
13880702	13880657		C1100, C1102	QTY 17 RADAR:8837828

C1100, C1102, C1103, C1117, C1144, C1165, C1156, C1158, C1172, C11615, C1621, C1715,

SYNC MASTER=MIKE SYNC DATE=N/A

AP: POWER

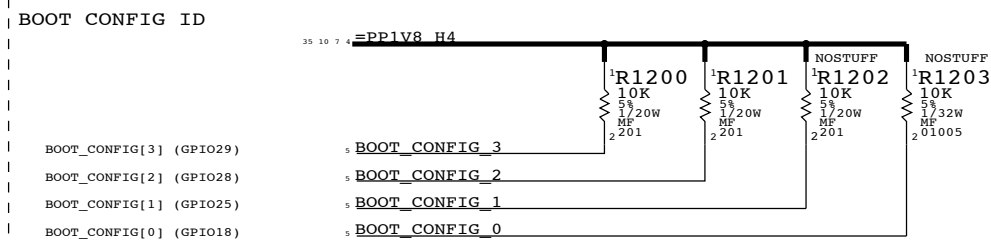
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DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

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PAGE: 11 OF 157 SHEET: 9 OF 48

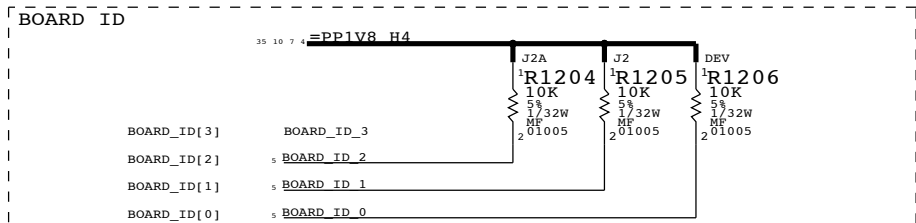


BOOT_CONFIG[3-0]

1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

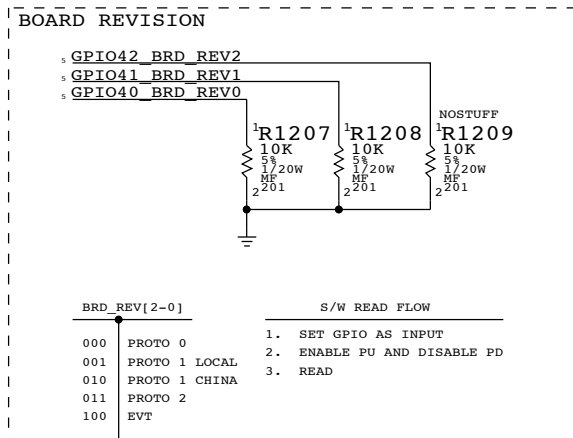


BOARD_ID[3-0]

0000	J1 AP
0001	J1 DEV
0010	J2 AP
0011	J2 DEV
0100	J2A AP
0101	J2A DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

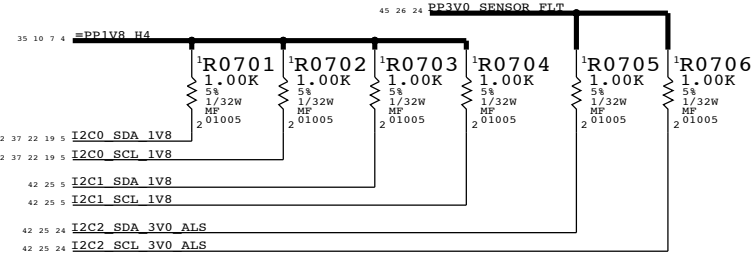


FOR REFERENCE

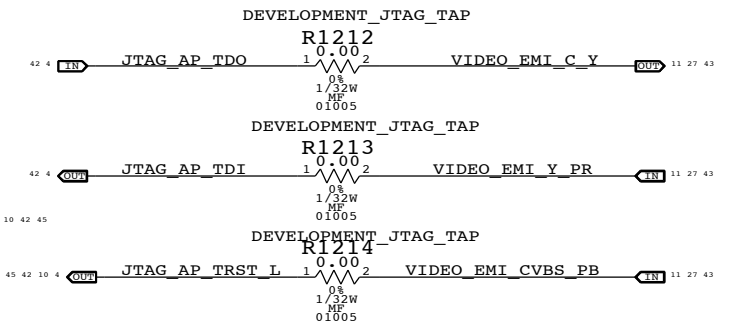
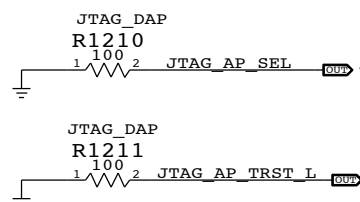
0000	SPIO
0001	SPI1
0010	SPIO W/TEST
0011	SPI1 W/TEST
0100	FMIO 2CS
0101	FMIO 4CS
0110	FMIO 4CS W/TEST
0111	RESERVED
1000	FMIO 2 CS
1001	FMIO 4 CS
1010	FMIO 4CS W/TEST
1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS W/TEST
1111	RESERVED

CURRENT SETTING ->

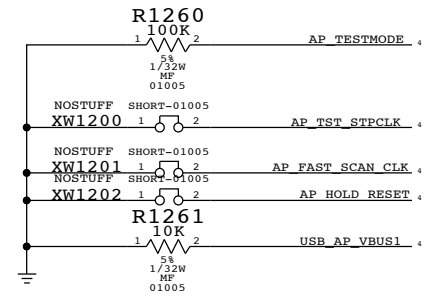
I2C PULL-UPS



JTAG



2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG	DEVELOPMENT_JTAG	JTAG_DAP
JTAG_DAP	DEVELOPMENT_JTAG_TAP	



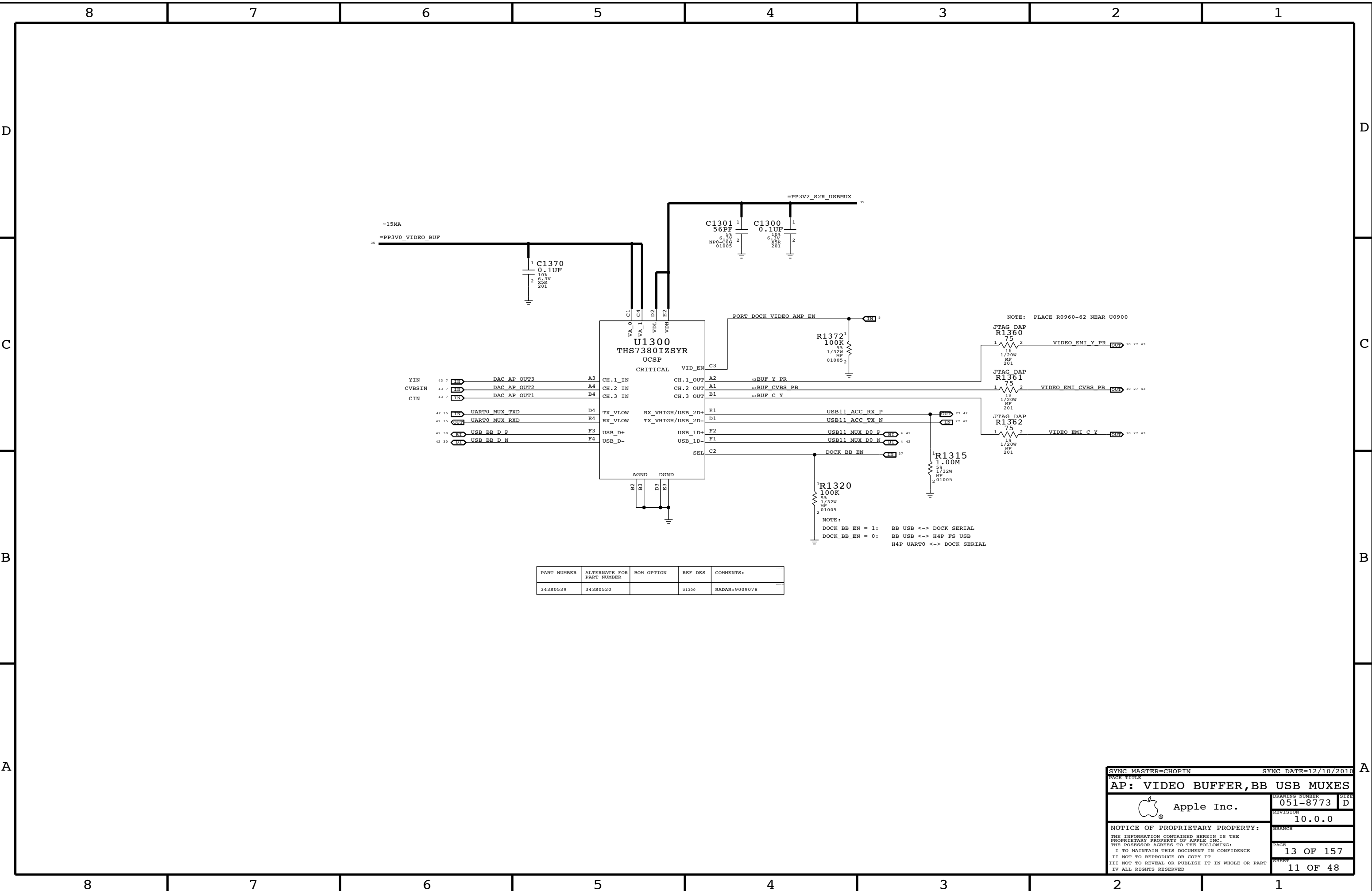
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AP: MISC & ALIASES

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DRAWING NUMBER	051-8773	SIZE	D
REVISION	10.0.0	BRANCH	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
34380539	34380520		U1300	RADAR:9009078

SYNC MASTER=CHOPIN SYNC DATE=12/10/2010

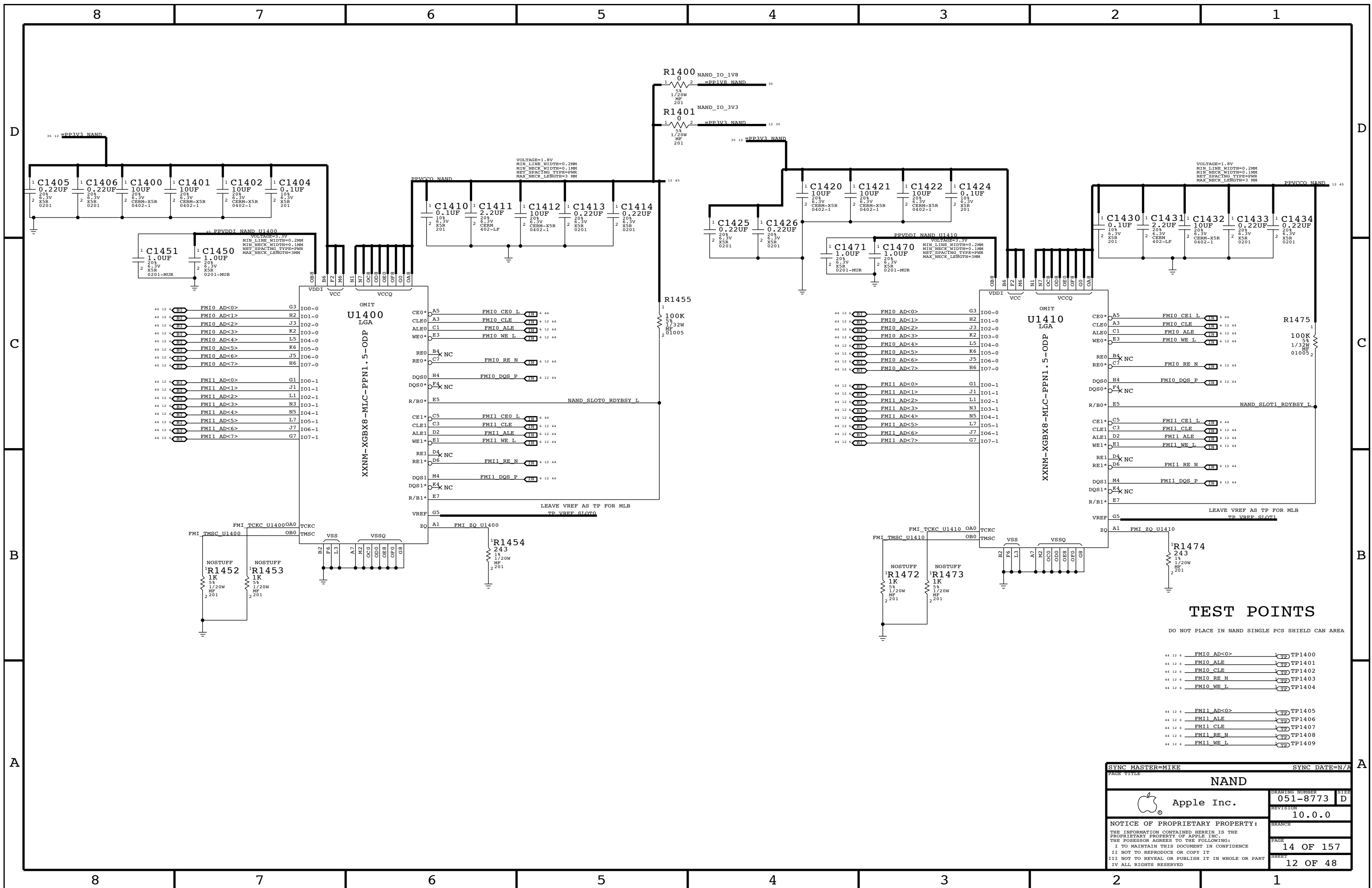
PAGE TITLE
AP: VIDEO BUFFER, BB USB MUXES

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PAGE: 13 OF 157
SHEET: 11 OF 48



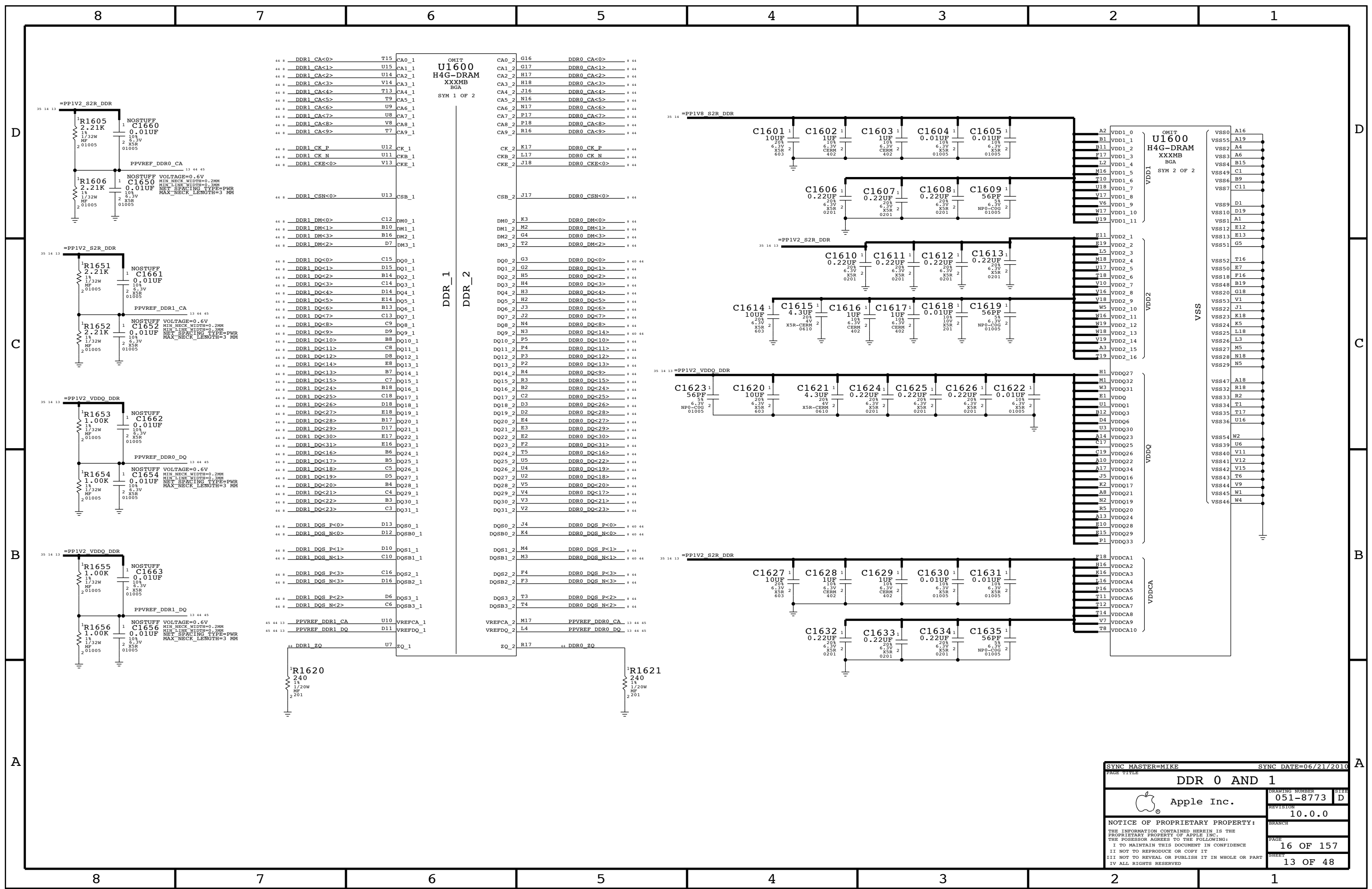
TEST POINTS

DO NOT PLACE IN NAND SINGLE PCS SHIELD CAN AREA

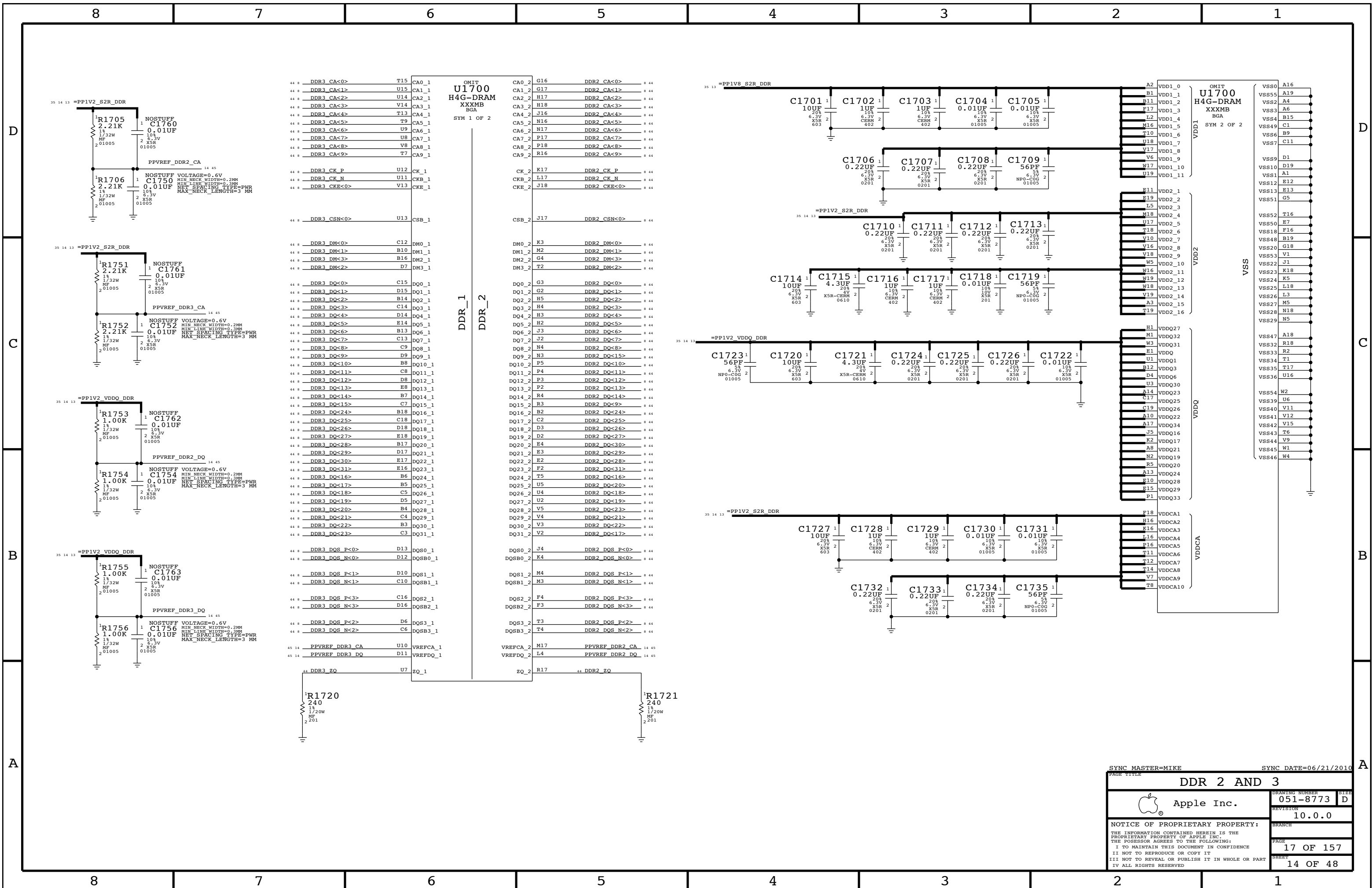
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- 44 12 6 FMIO ALE TP1401
- 44 12 6 FMIO CLE TP1402
- 44 12 6 FMIO RE_N TP1403
- 44 12 6 FMIO WE_L TP1404

- 44 12 6 FMII AD<0> TP1405
- 44 12 6 FMII ALE TP1406
- 44 12 6 FMII CLE TP1407
- 44 12 6 FMII RE_N TP1408
- 44 12 6 FMII WE_L TP1409

SYNC MASTER=MIKE		SYNC DATE=N/A	
NAND			
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		12 OF 48	
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PAGE TITLE			
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OMIT U1700 H4G-DRAM XXXMB BGA SYM 1 OF 2

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44	DDR3_CK_N	U11	CKB_1	CKB_2	L17	DDR2_CK_N	44
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45	PPVREF_DDR3_DQ	D11	VREFDQ_1	VREFDQ_2	L4	PPVREF_DDR2_DQ	14 45
44	DDR3_ZQ	U7	ZQ_1	ZQ_2	R17	DDR2_ZQ	44

SYNC MASTER=MIKE SYNC DATE=06/21/2010

DDR 2 AND 3

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

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WIFI ALIASES

42 40 4	<u>HSIC1 WLAN DATA1</u>	<u>HSIC DATA 4330</u>	31 33
42 40 4	<u>HSIC1 WLAN STB1</u>	<u>HSIC STROBE 4330</u>	31 33
42 5	<u>HSIC HOST READY WLAN</u>	<u>WLAN GPIO1</u>	31 33
42 5	<u>HSIC WLAN_RDY</u>	<u>HSIC_DEVICE_READY</u>	31
42 37	<u>RST WLAN_L</u>	<u>WLAN_ENABLE</u>	31 33
37	<u>PM WLAN HOST WAKE</u>	<u>WLAN_GPIO0</u>	31 33
42 37	<u>RST_BT_L</u>	<u>BT RESET_N</u>	31 33
37	<u>PM_BT_HOST WAKE</u>	<u>BT_HOST WAKE</u>	31 33
5	<u>PM_BT WAKE</u>	<u>BT WAKE</u>	31 33
42 5	<u>UART3_BT_RXD</u>	<u>BT_UART_TXD</u>	31 33
42 5	<u>UART3_BT_TXD</u>	<u>BT_UART_RXD</u>	31 33
42 5	<u>UART3_BT_CTS_L</u>	<u>BT_UART_RTS_N</u>	31 33
42 5	<u>UART3_BT_RTS_L</u>	<u>BT_UART_CTS_N</u>	31 33
42 37	<u>CLK_32K WLAN</u>	<u>CLK32K</u>	32 33
42 19 5	<u>I2S2_VSP_BCLK</u>	<u>BT_PCM_CLK</u>	31
42 19 5	<u>I2S2_VSP_DOUT</u>	<u>BT_PCM_DIN</u>	31
42 19 5	<u>I2S2_VSP_DIN</u>	<u>BT_PCM_DOUT</u>	31
42 19 5	<u>I2S2_VSP_LRCK</u>	<u>BT_PCM_SYNC</u>	31
42 5	<u>UART6 WLAN_RXD</u>	<u>WLAN_GPIO4</u>	31 33
42 5	<u>UART6 WLAN_TXD</u>	<u>WLAN_GPIO3</u>	31 33


UART ALIASES

42 5	<u>UART0_AP_RXD</u>	<u>UART0_MUX_RXD</u>	11 42
42 5	<u>UART0_AP_TXD</u>	<u>UART0_MUX_TXD</u>	11 42

OBSOLETE ALIASES

<u>NC_EXT_SMPS_REQ</u>	<u>EXT_SMPS_REQ</u>	31
<u>NC_EXT_PWM_REQ</u>	<u>EXT_PWM_REQ</u>	31
<u>NC_BT_GPIO5</u>	<u>BT_GPIO5</u>	31
<u>TP_WLAN_GPIO5</u>	<u>WLAN_GPIO5</u>	31

42 30 5 GSM_TXBURST_IND LED_DRIVE_GSMB
 NEED TO DOUBLE CHECK IF WE NEED THIS IN IPAD, OR IF THIS MIGHT BE A PHONE SPECIFIC ISSUE

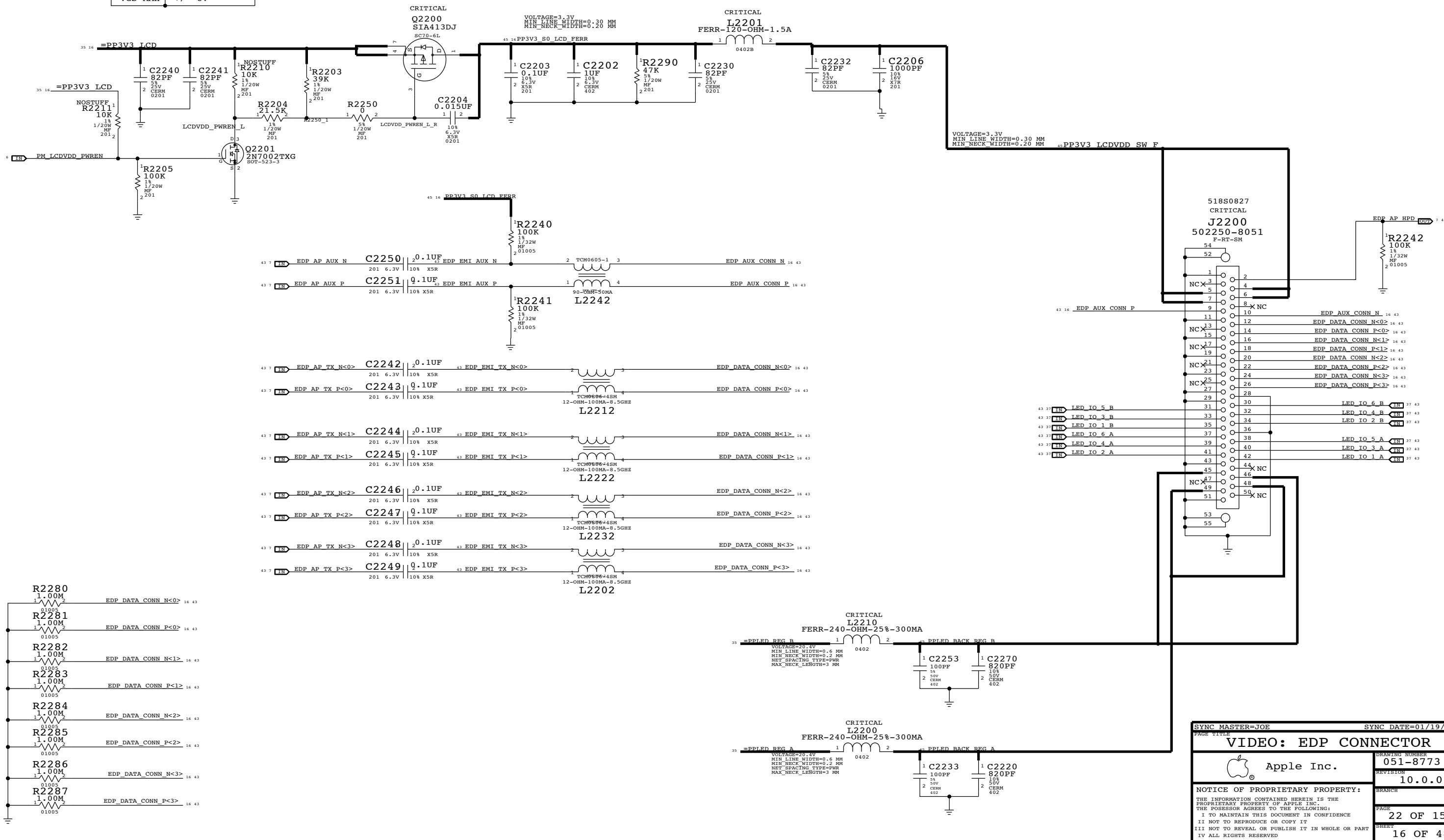
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MLB ALIASES/CONNECTIONS			
 Apple Inc.		DRAWING NUMBER	051-8773
		REVISION	10.0.0
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EDP CONNECTOR

SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

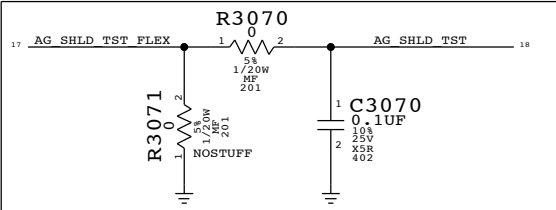
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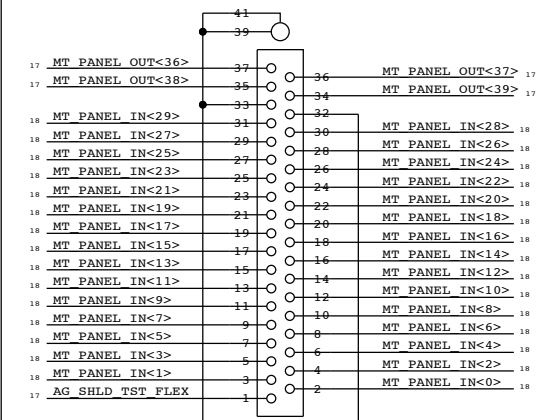
SYNC MASTER=JOE		SYNC DATE=01/19/2011	
PAGE TITLE			
VIDEO: EDP CONNECTOR			
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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CONNECTORS TO GRAPE FLEX

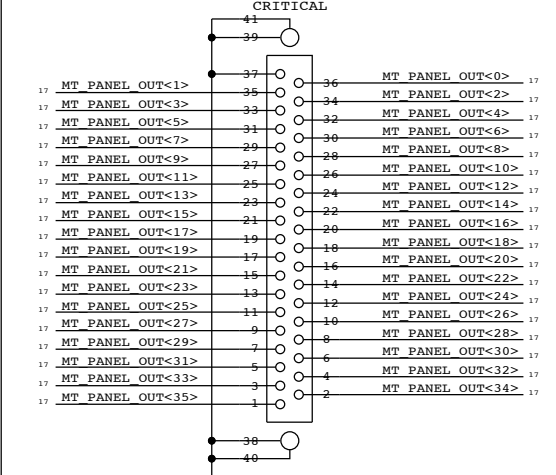


CRITICAL
P/N 518S0828



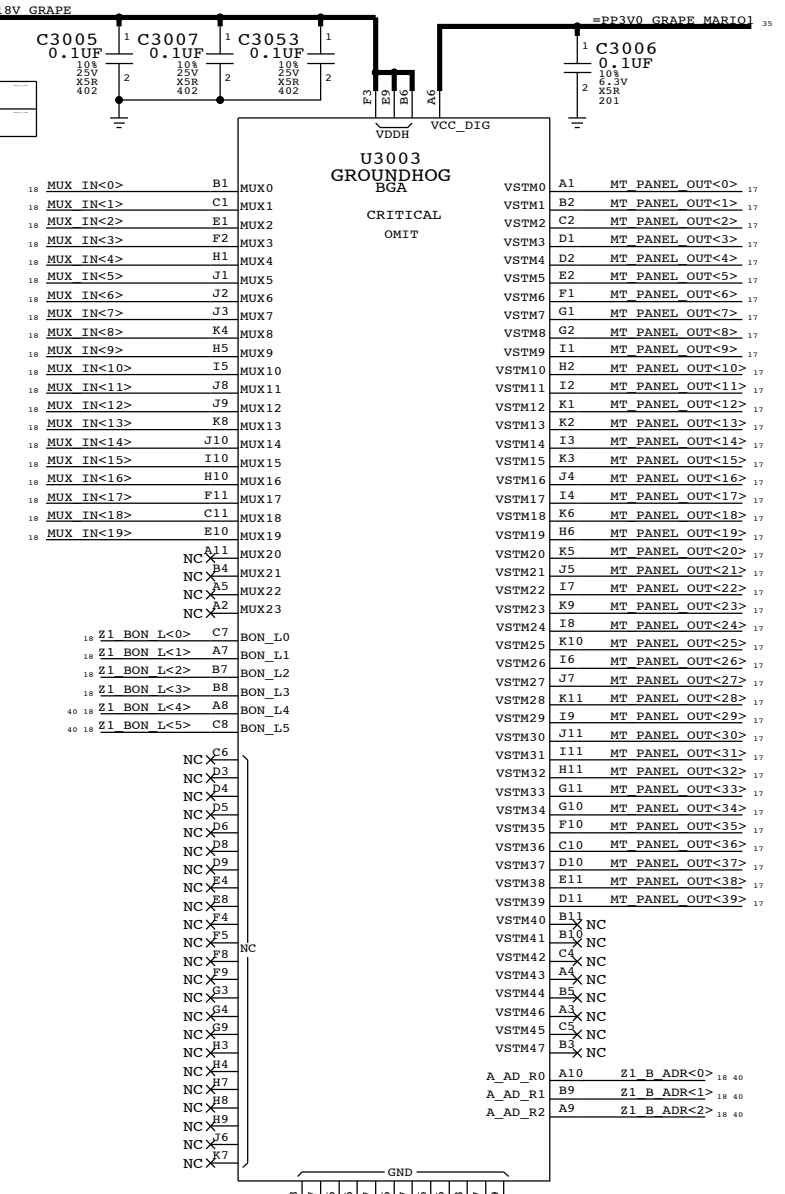
F-RT-SM
502250-8037
J3010

MATES WITH LEFTMOST GRAPE FLEX TAIL

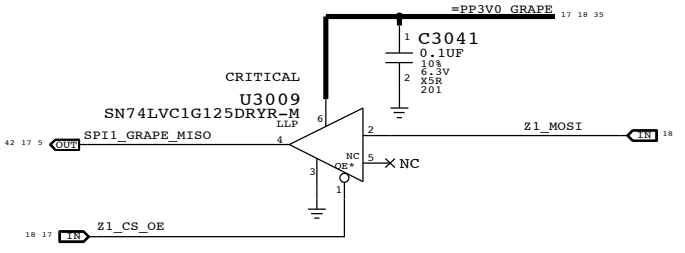
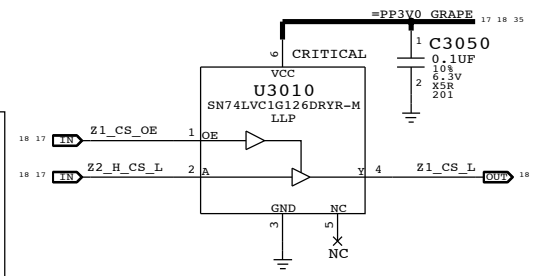
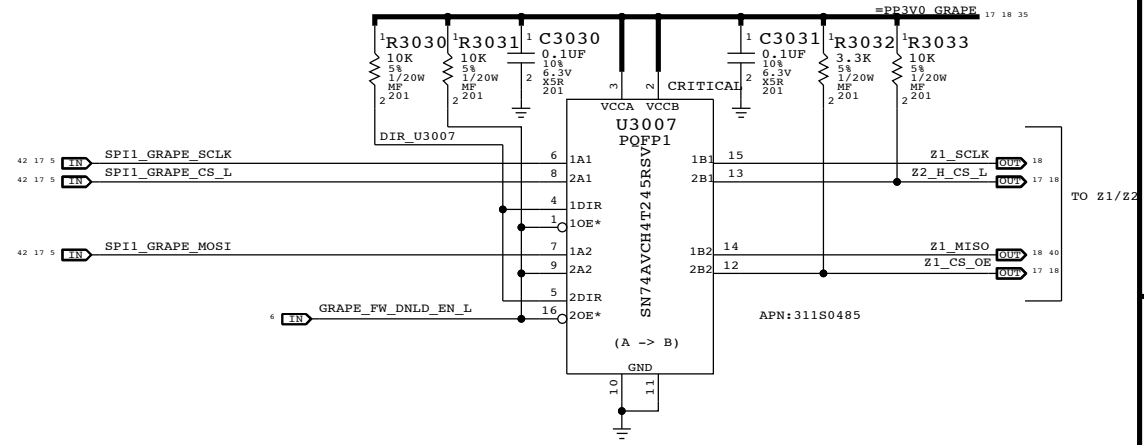
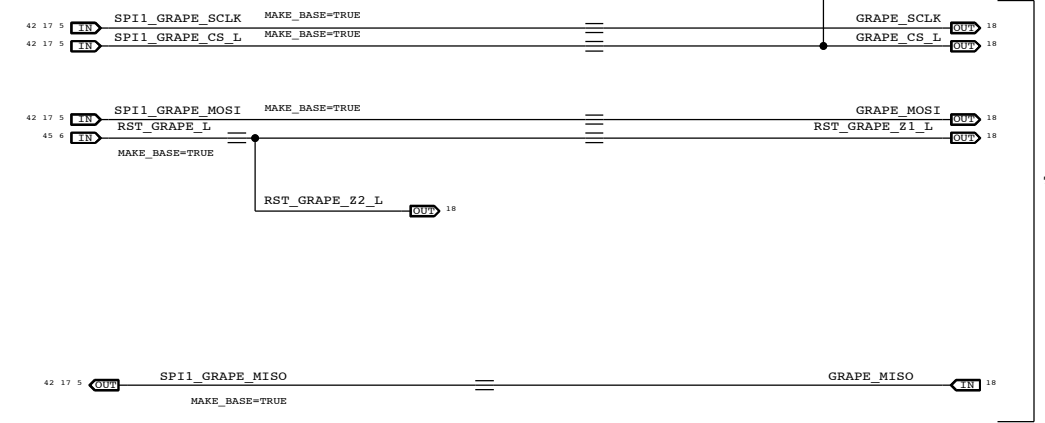
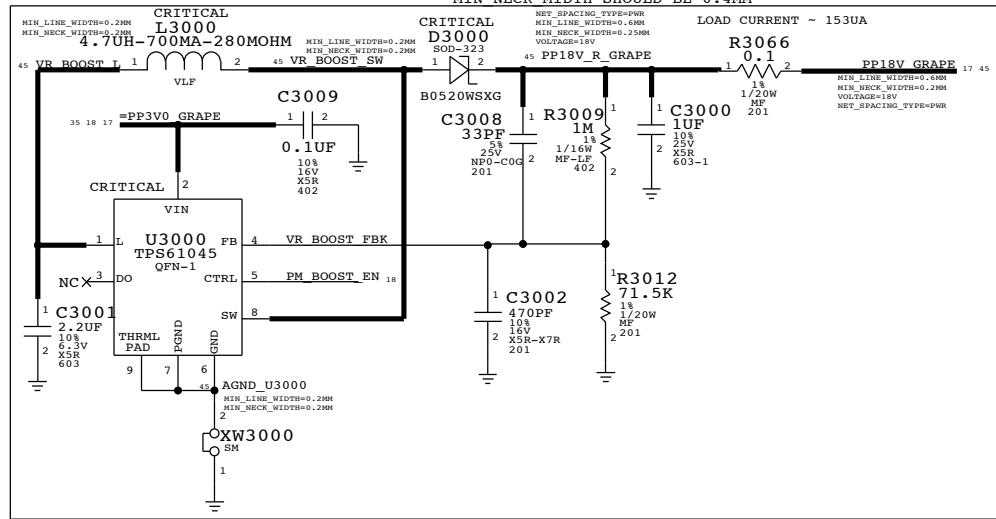


F-RT-SM
502250-8037
J3011

MATES WITH RIGHTMOST GRAPE FLEX TAIL



BOOST CONVERTOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31180523	31180485		U3007	
31180524	31180533		U3009	
31180525	31180532		U3010	

SYNC MASTER=RAMSIN SYNC DATE=12/17/2010

GRAPE: GROUNDHOG, CONN, BOOST

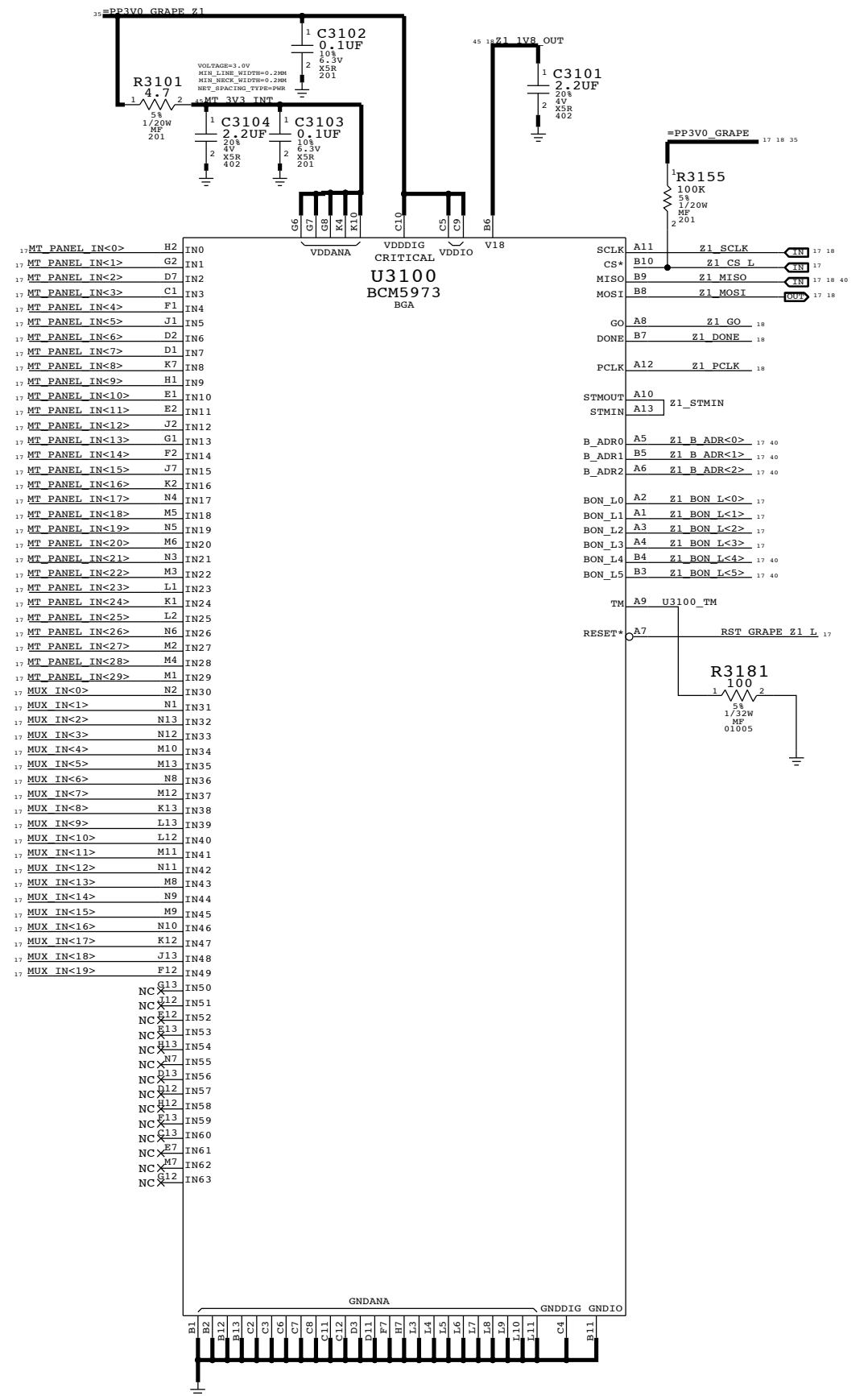
Apple Inc.

DRAWING NUMBER: 051-8773
REVISION: 10.0.0

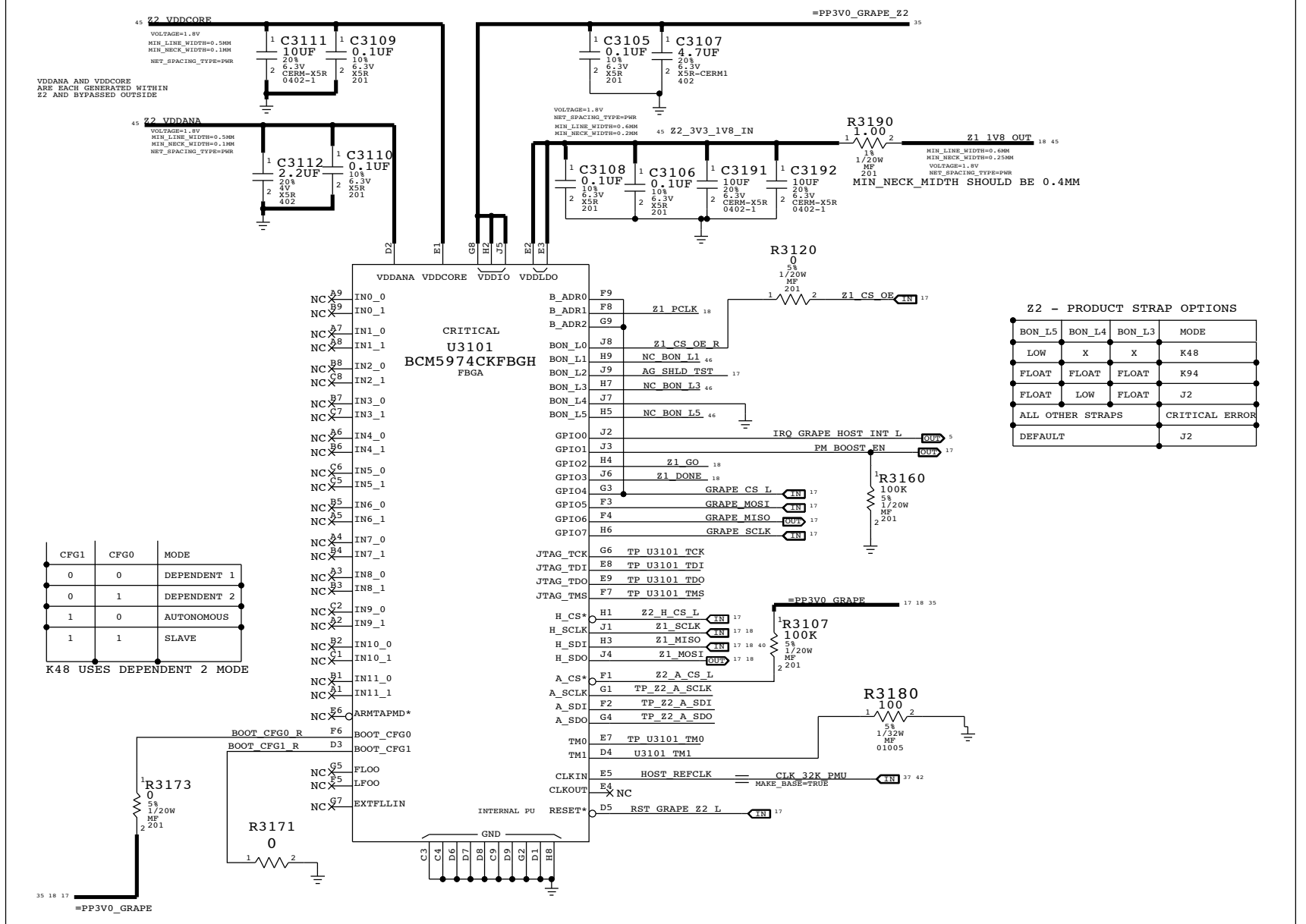
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PAGE: 30 OF 157
SHEET: 17 OF 48

ZEPHYR 1+ ASIC



ARM9 MCU (Z2 BASED)



SYNC MASTER=RAMSIN SYNC DATE=12/17/2010

GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

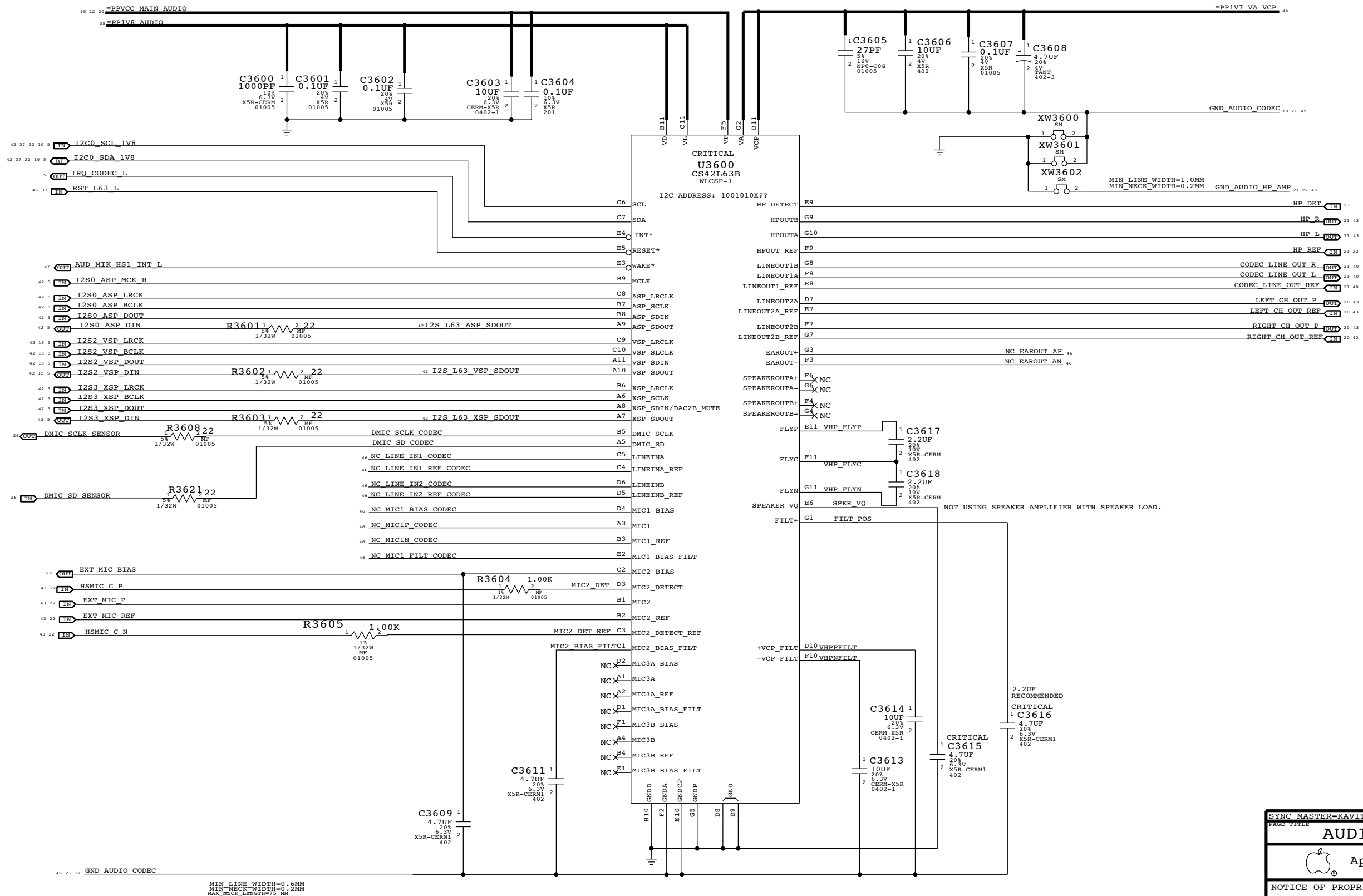
REVISION: 10.0.0

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L63B AUDIO CODEC

APN:338S0940



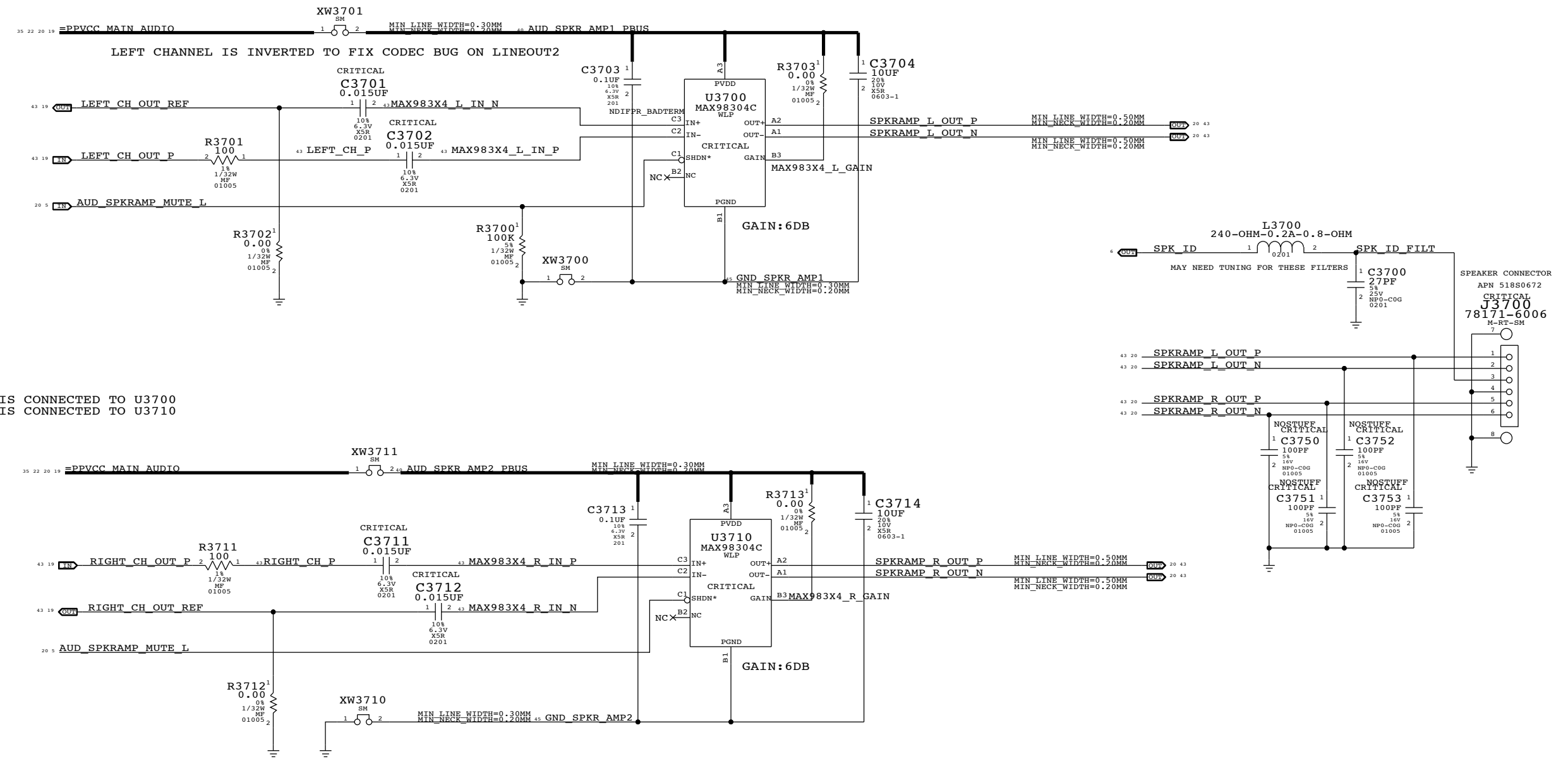
MIN LINE WIDTH=0.6MM
MIN NECK WIDTH=0.2MM
MAX NECK LENGTH=75 MM

SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
PAGE TITLE			
AUDIO: L63B CODEC			
DRAWING NUMBER		SIZE	
051-8773		D	
REVISION		PAGE	
10.0.0		36 OF 157	
BRANCH		SHEET	
		19 OF 48	
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SPEAKER AMPLIFIER

APN:353S3317)
 TURN ON TIME: 3.5MS
 75HZ +/- XXX%
 TURN ON DELAY: ?MS

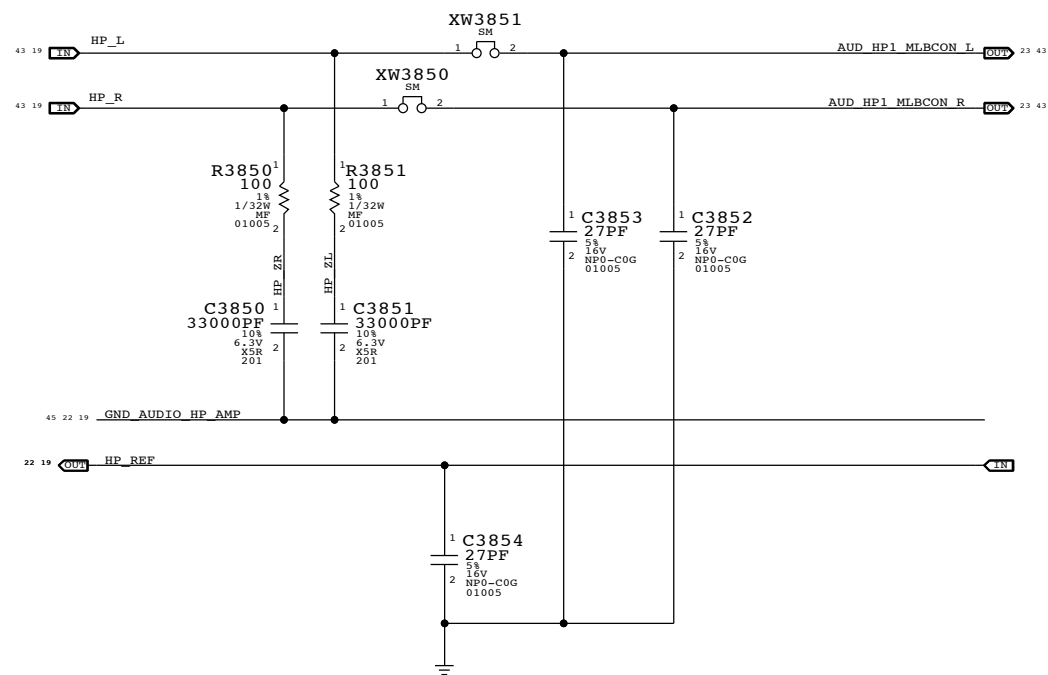
GAIN	VDD	GND
12DB	NC	SHORT
9DB	NC	100K
6DB	SHORT	NC
3DB	100K	NC
0DB	NC	NC



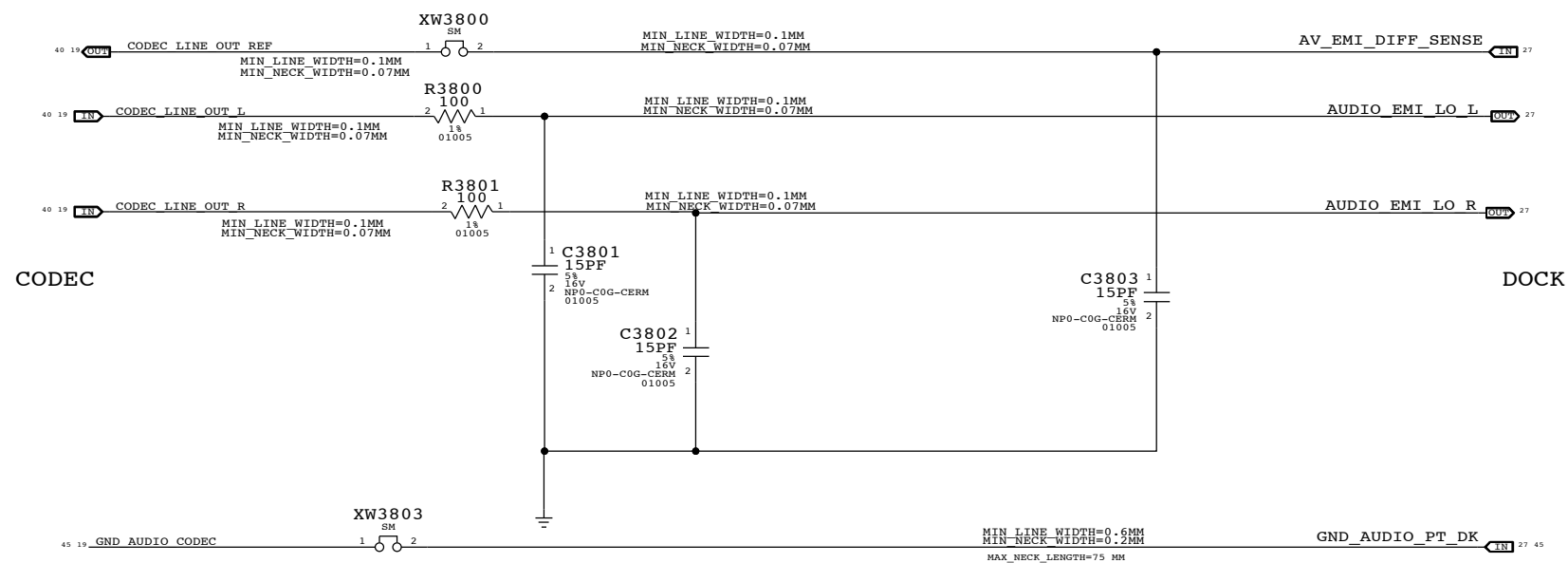
L63 LINEOUT2A IS CONNECTED TO U3700
 L63 LINEOUT2B IS CONNECTED TO U3710

SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
AUDIO: SPEAKER AMP			
Apple Inc.		DRAWING NUMBER	051-8773
		REVISION	10.0.0
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I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	20 OF 48
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HEADPHONE OUTPUT ZOBEL NETWORK

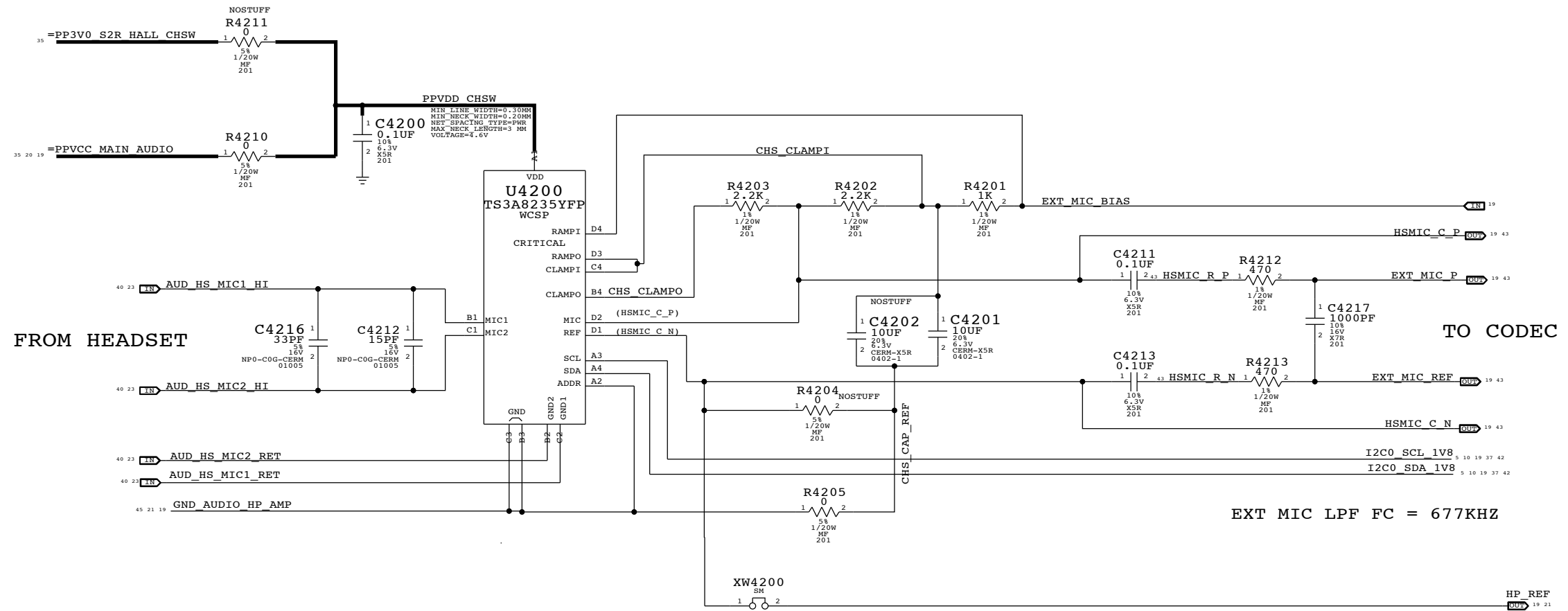


DOCK LINE OUTPUT



SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
AUDIO: HEADPHONE OUT			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8773	D
		REVISION	
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		PAGE	38 OF 157
		SHEET	21 OF 48

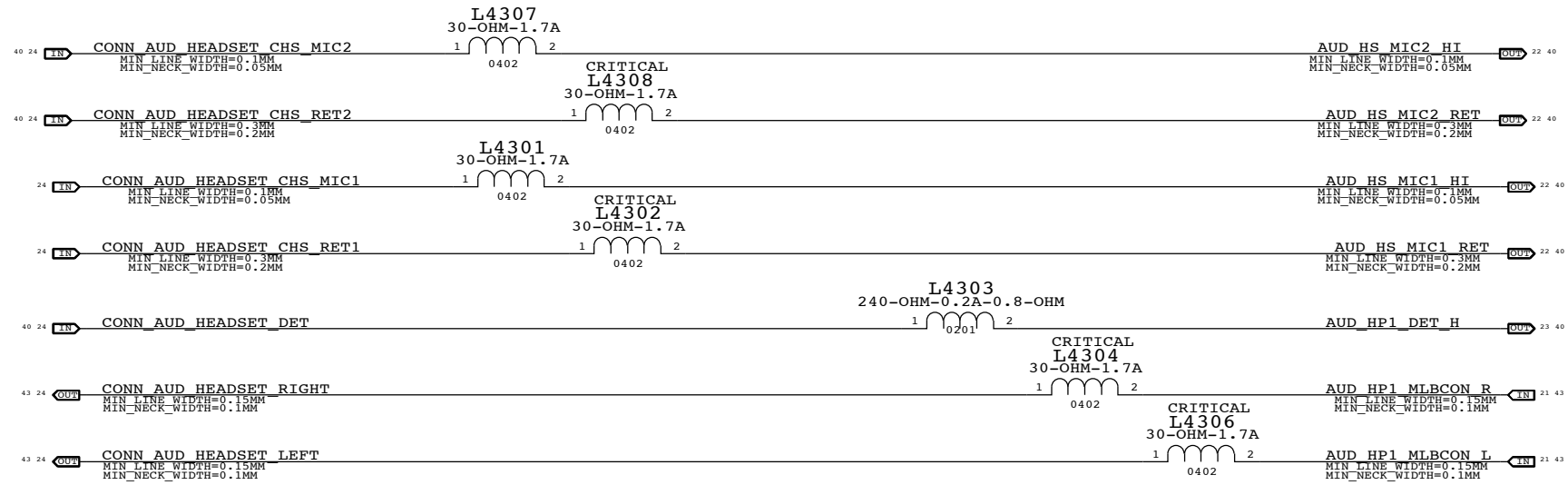
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



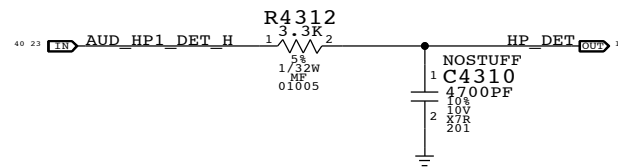
SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
PAGE TITLE			
AUDIO: DETECT/MIC BIAS			
DRAWING NUMBER		SIZE	
051-8773		D	
REVISION		PAGE	
10.0.0		42 OF 157	
BRANCH		SHEET	
		22 OF 48	
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HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29

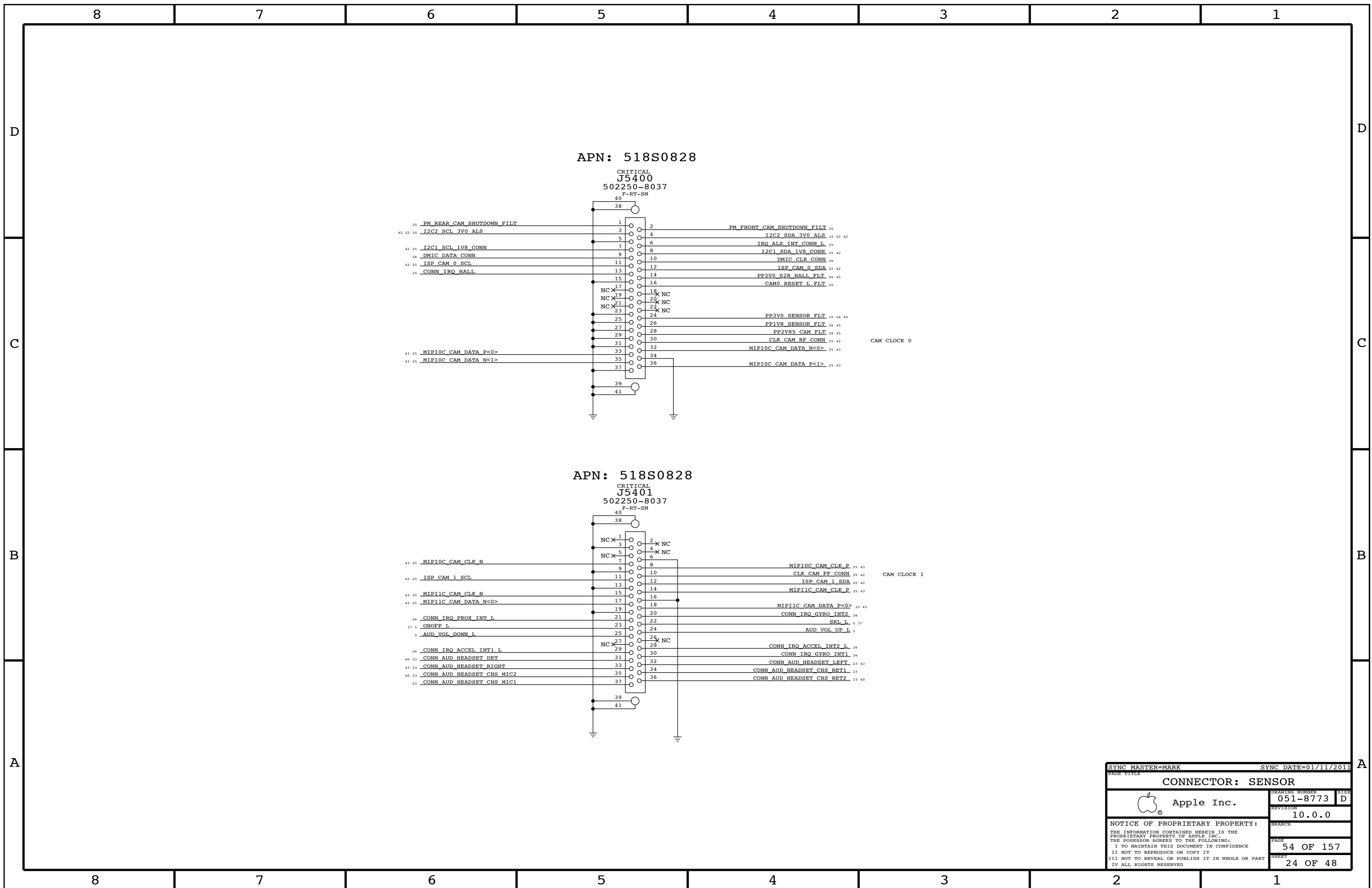
PLACE ALL COMPONENTS NEAR J5401



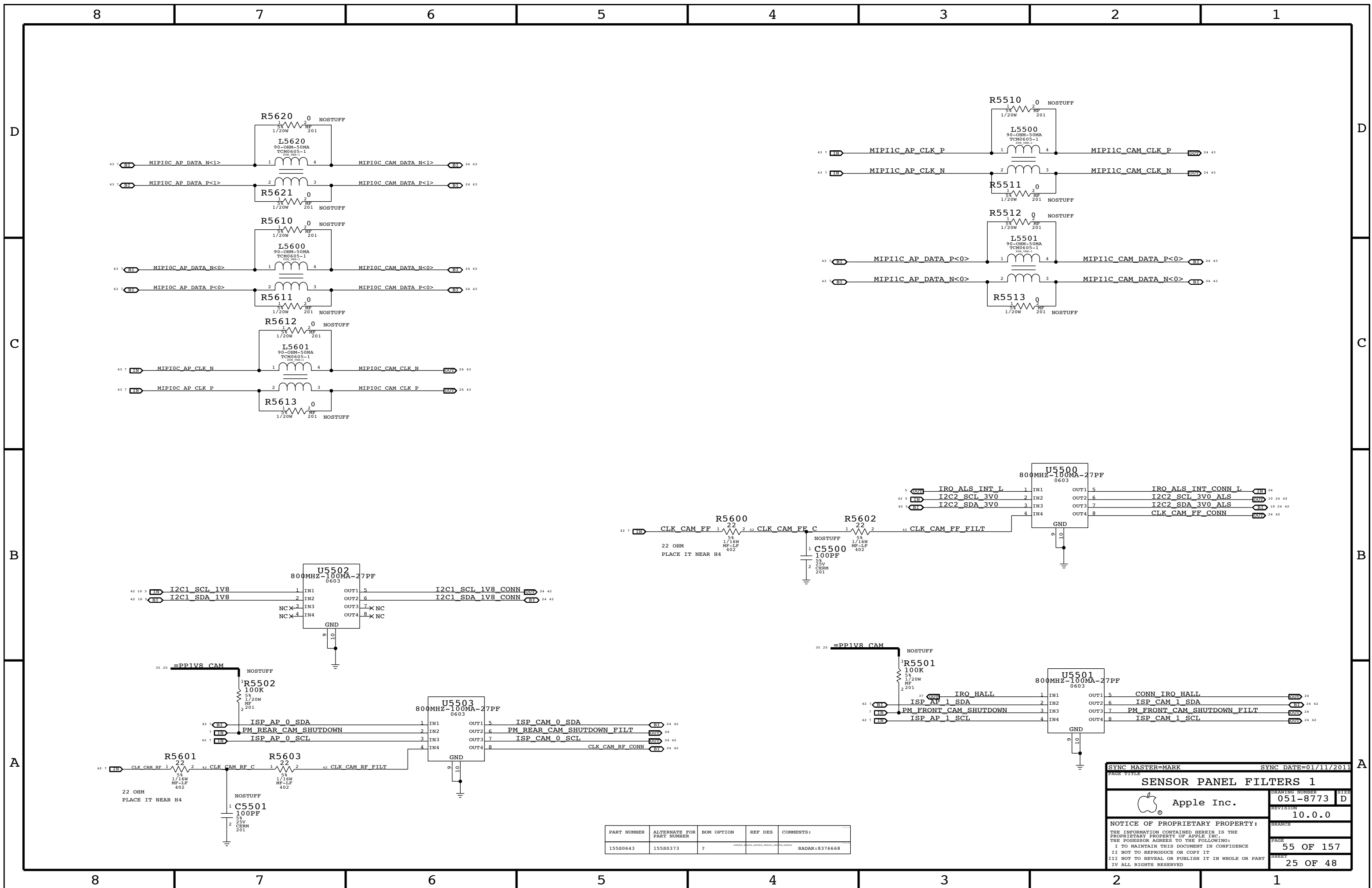
HEADSET JACK INSERTION DETECT



SYNC MASTER=KAVITHA		SYNC DATE=02/03/2011	
PAGE TITLE AUDIO: HP/MIC FILTERS			
DRAWING NUMBER 051-8773		SIZE D	
REVISION 10.0.0		BRANCH	
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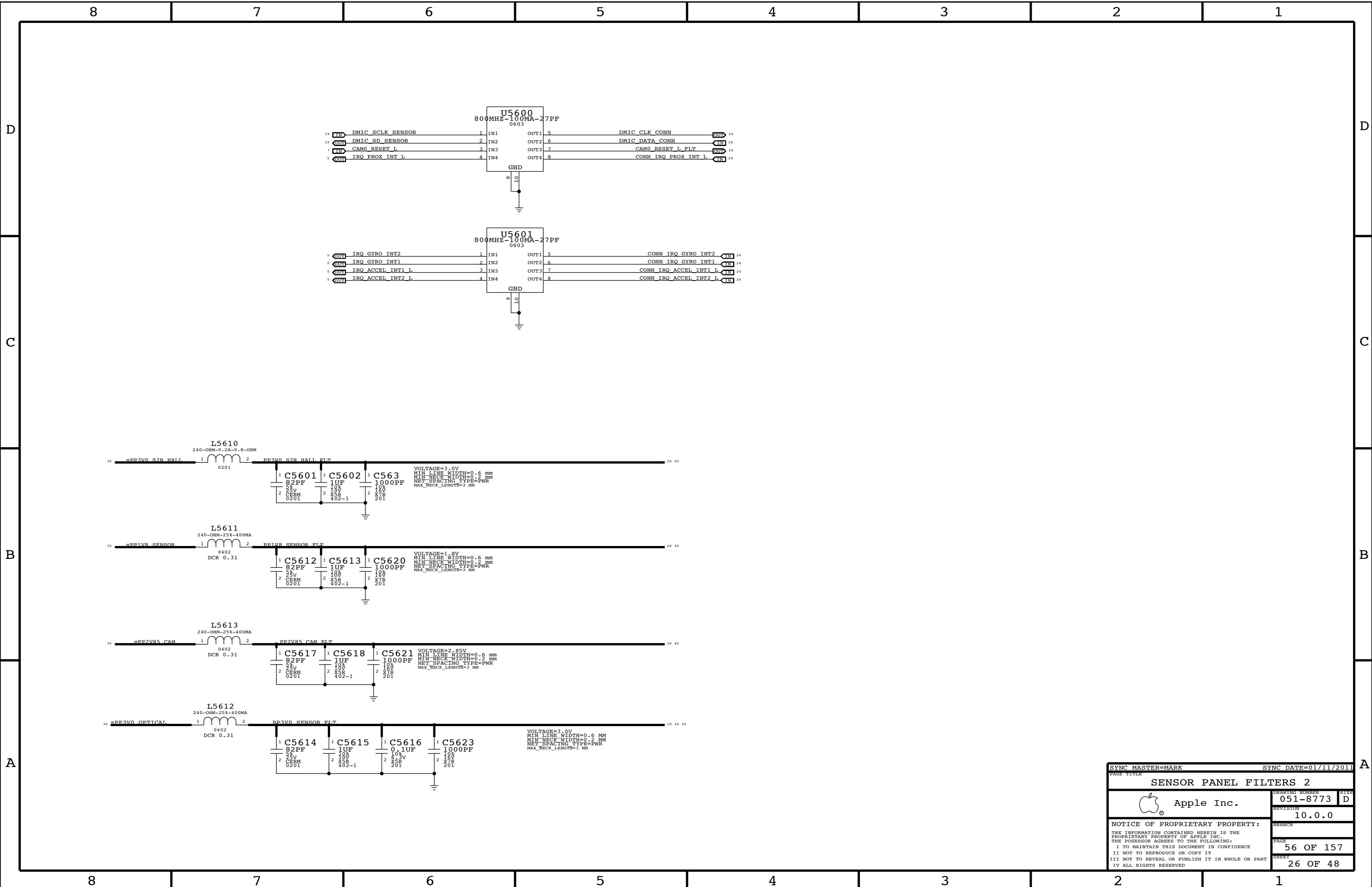


SYNC MASTER=MARK		SYNC DATE=01/11/2011	
PAGE TITLE			
CONNECTOR: SENSOR			
DRAWING NUMBER		051-8773	SIZE
REVISION		10.0.0	
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SHEET		24 OF 48	

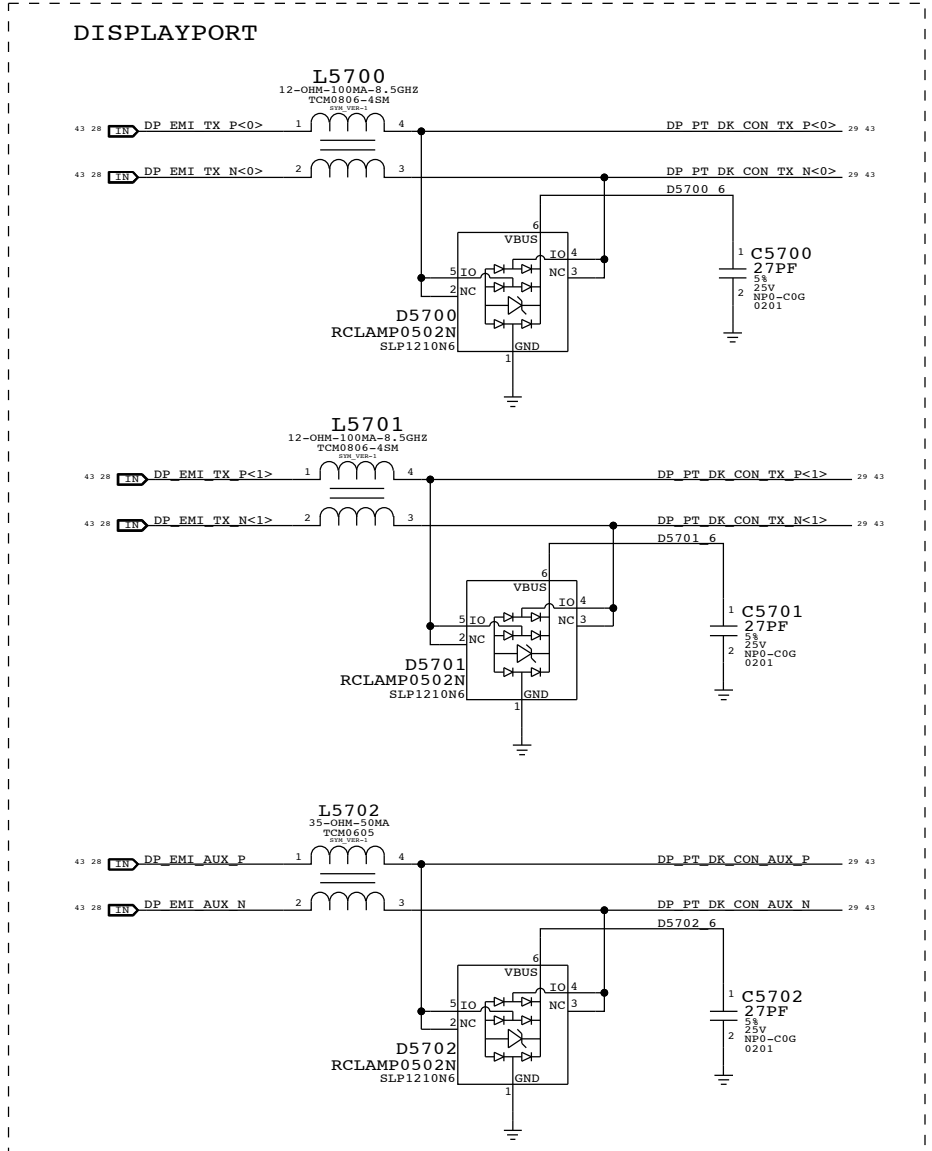
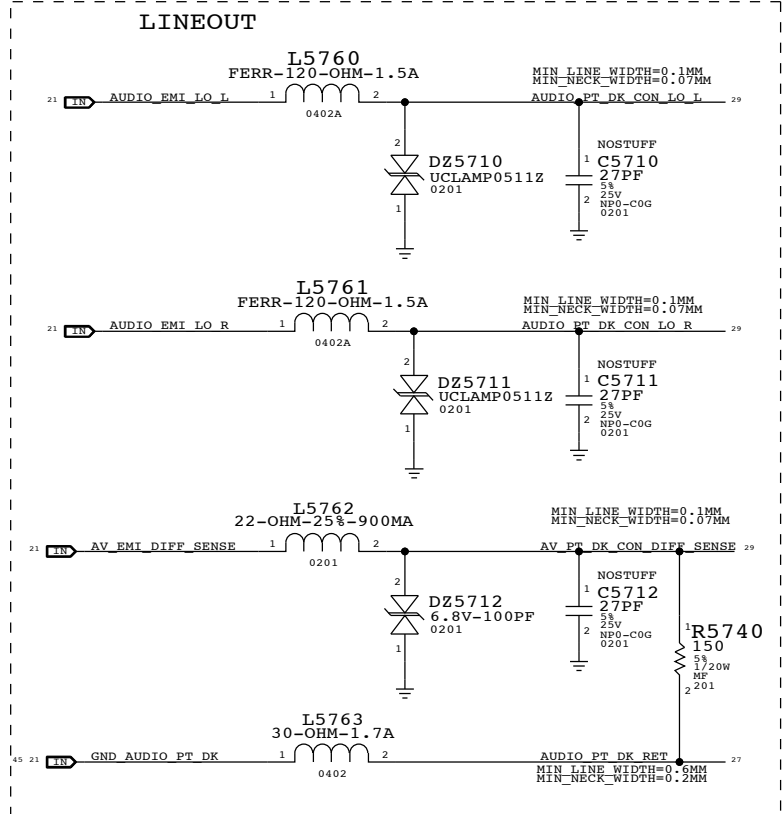
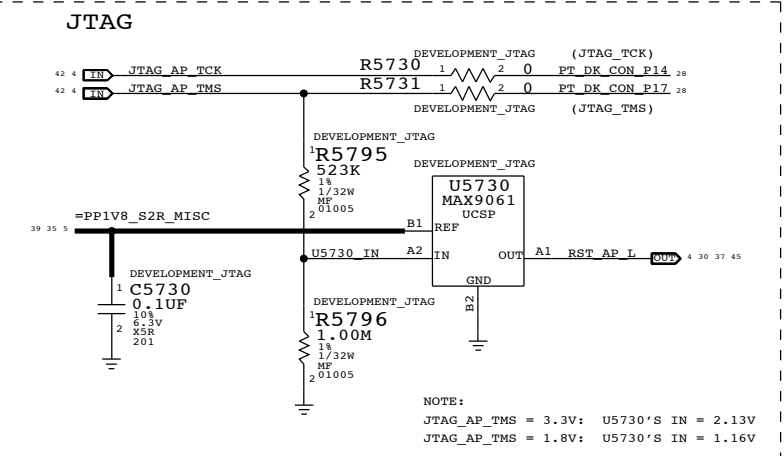
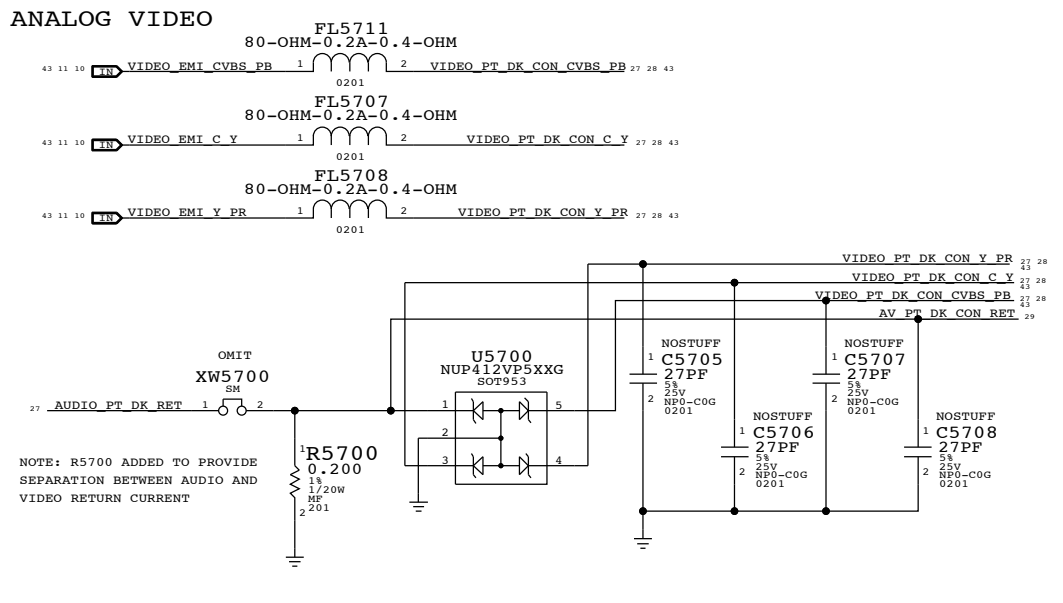
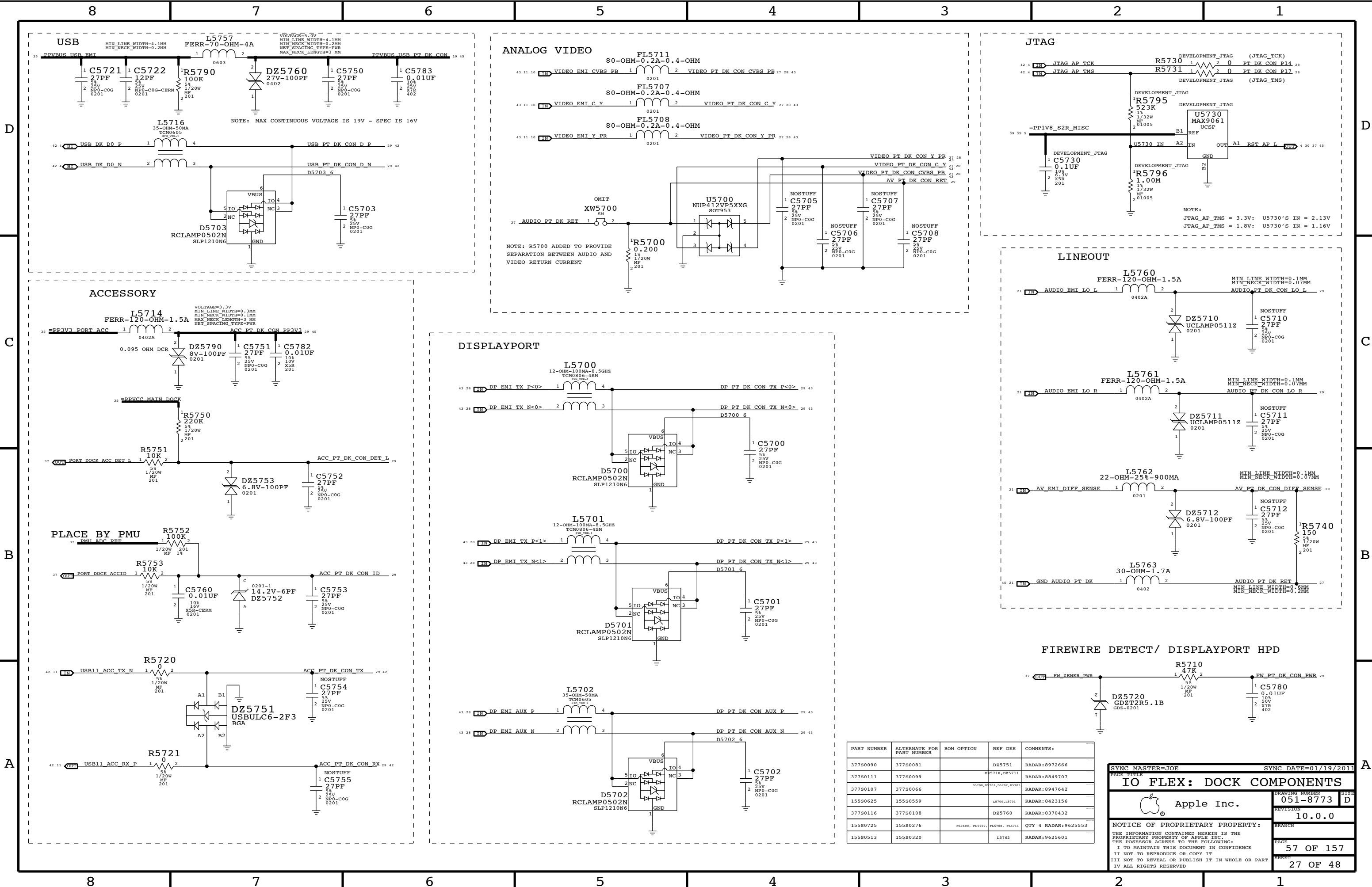


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0643	155S0373	?		RADAR:8376668

SYNC MASTER=MARK SYNC DATE=01/11/2011
SENSOR PANEL FILTERS 1
 Apple Inc.
 DRAWING NUMBER: 051-8773 SIZE: D
 REVISION: 10.0.0
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PAGE TITLE		SYNC MASTER=MARK		SYNC DATE=01/11/2011	
SENSOR PANEL FILTERS 2					
		DRAWING NUMBER		SIZE	
		051-8773		D	
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		10.0.0			
		PAGE		SHEET	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37780090	37780081		D25751	RADAR:8972666
37780111	37780099		D25710,D25711	RADAR:8849707
37780107	37780066		D5700,D5701,D5702,D5703	RADAR:8947642
15580625	15580559		L5700,L5701	RADAR:8423156
37780116	37780108		D25760	RADAR:8370432
15580725	15580276	FL0600, FL5707, FL5708, FL5711		QTY 4 RADAR:9625553
15580513	15580320		L5762	RADAR:9625601

SYNC MASTER=JOE SYNC DATE=01/19/2011

IO FLEX: DOCK COMPONENTS

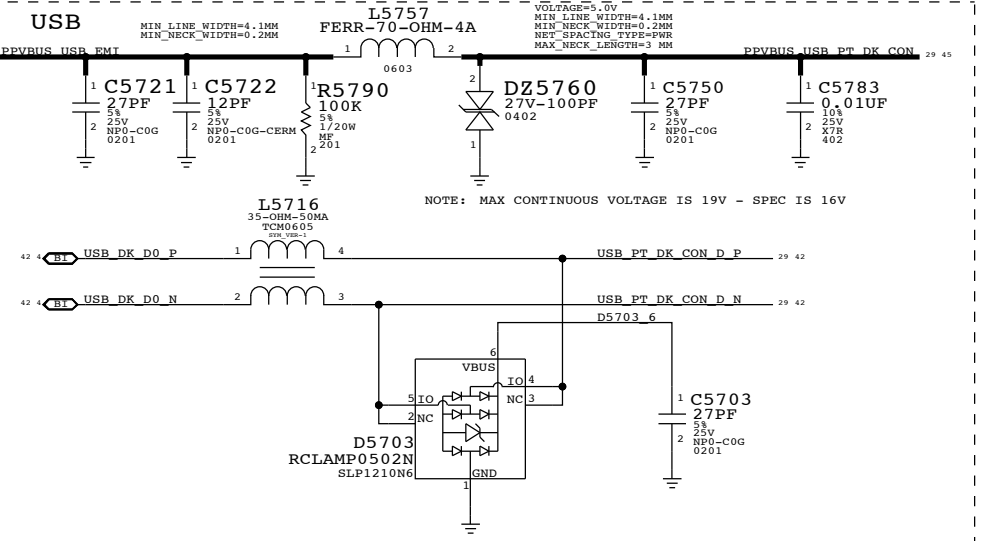
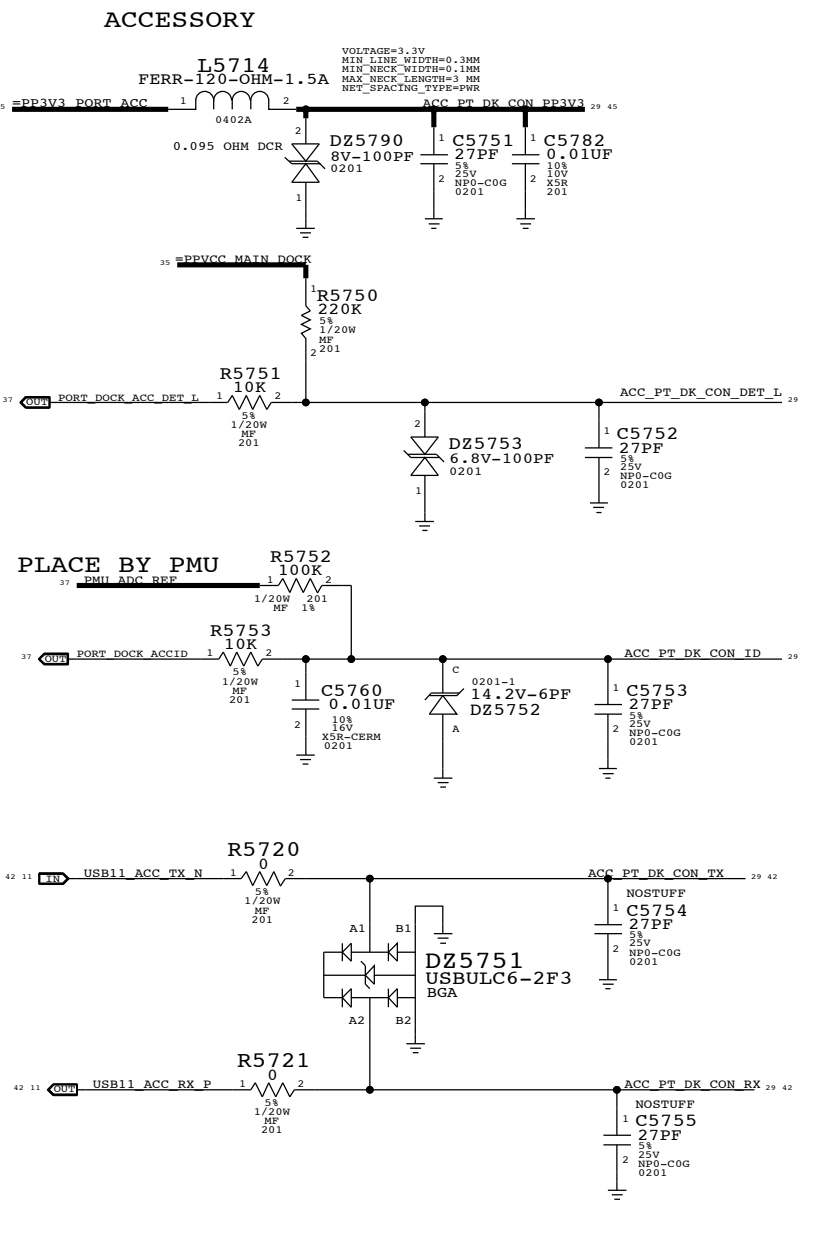
Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

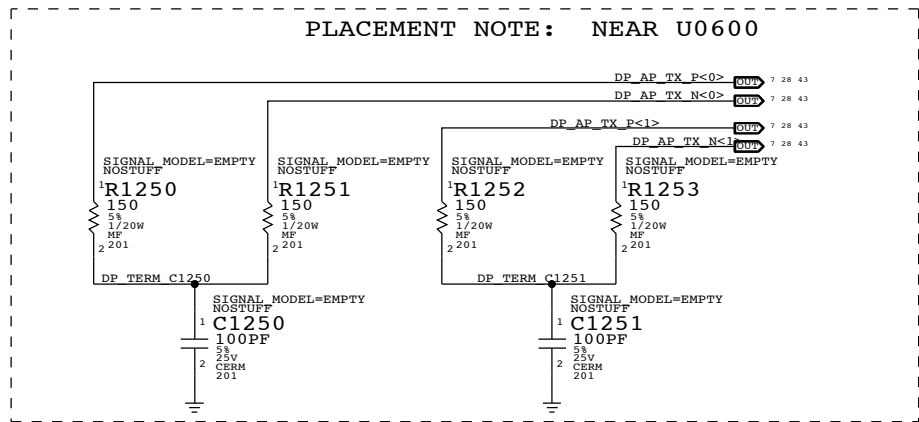
REVISION: 10.0.0

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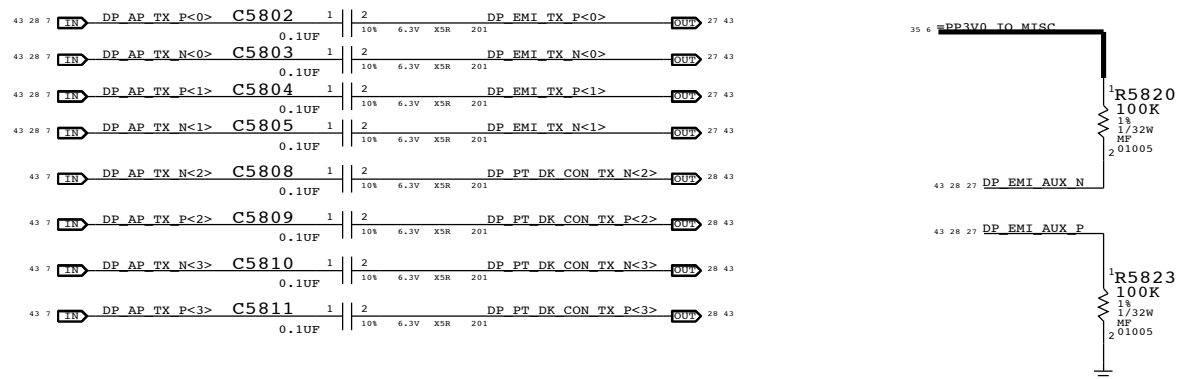
PAGE: 57 OF 157
SHEET: 27 OF 48



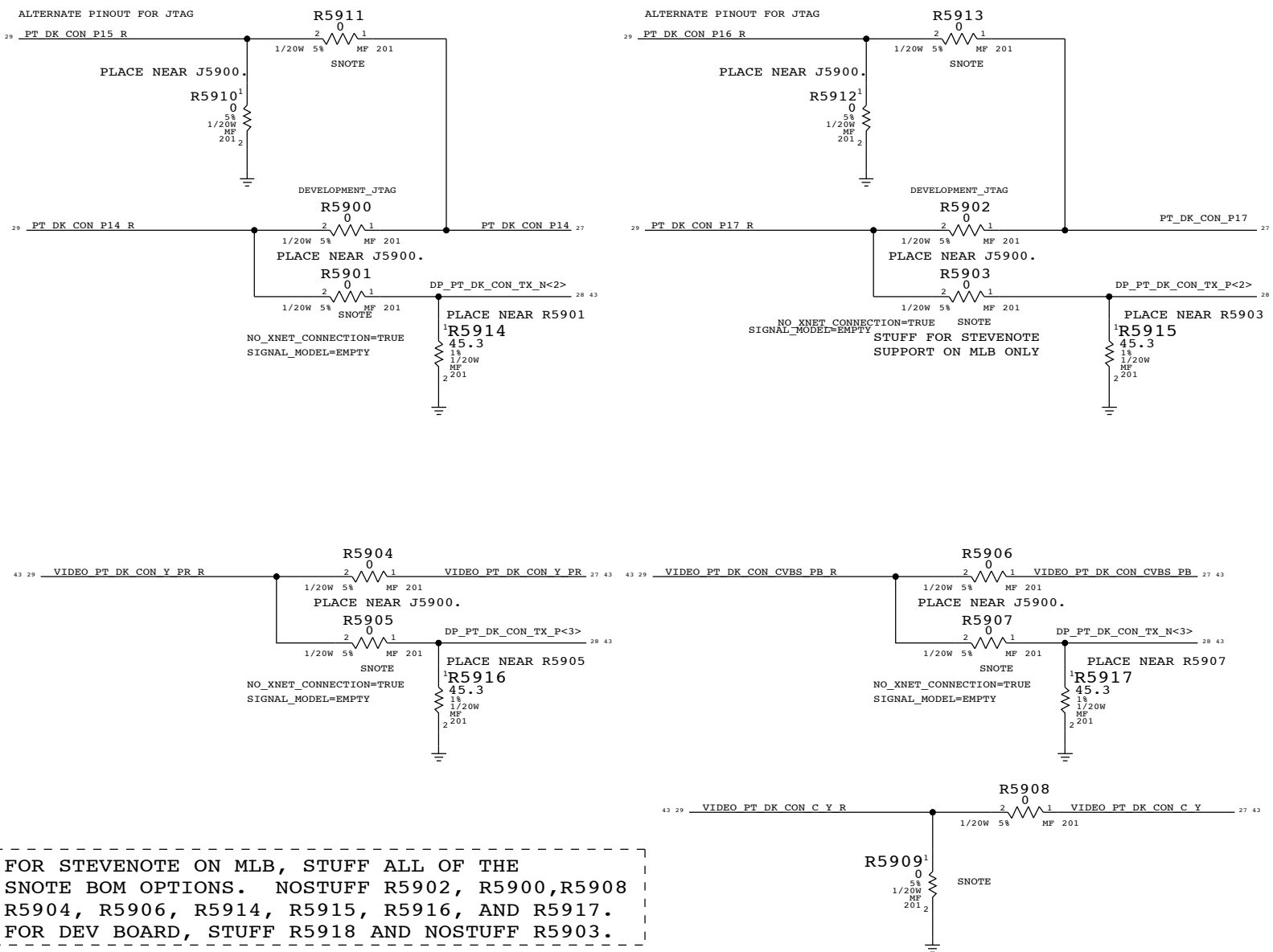
PLACEMENT NOTE: NEAR U0600



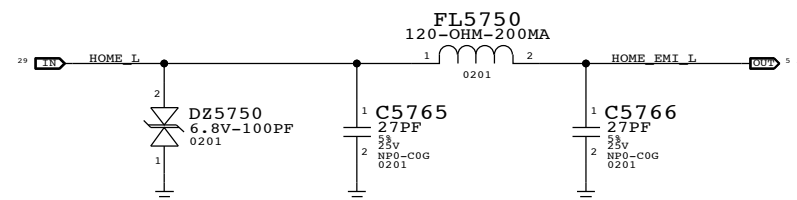
DISPLAYPORT AC COUPLING



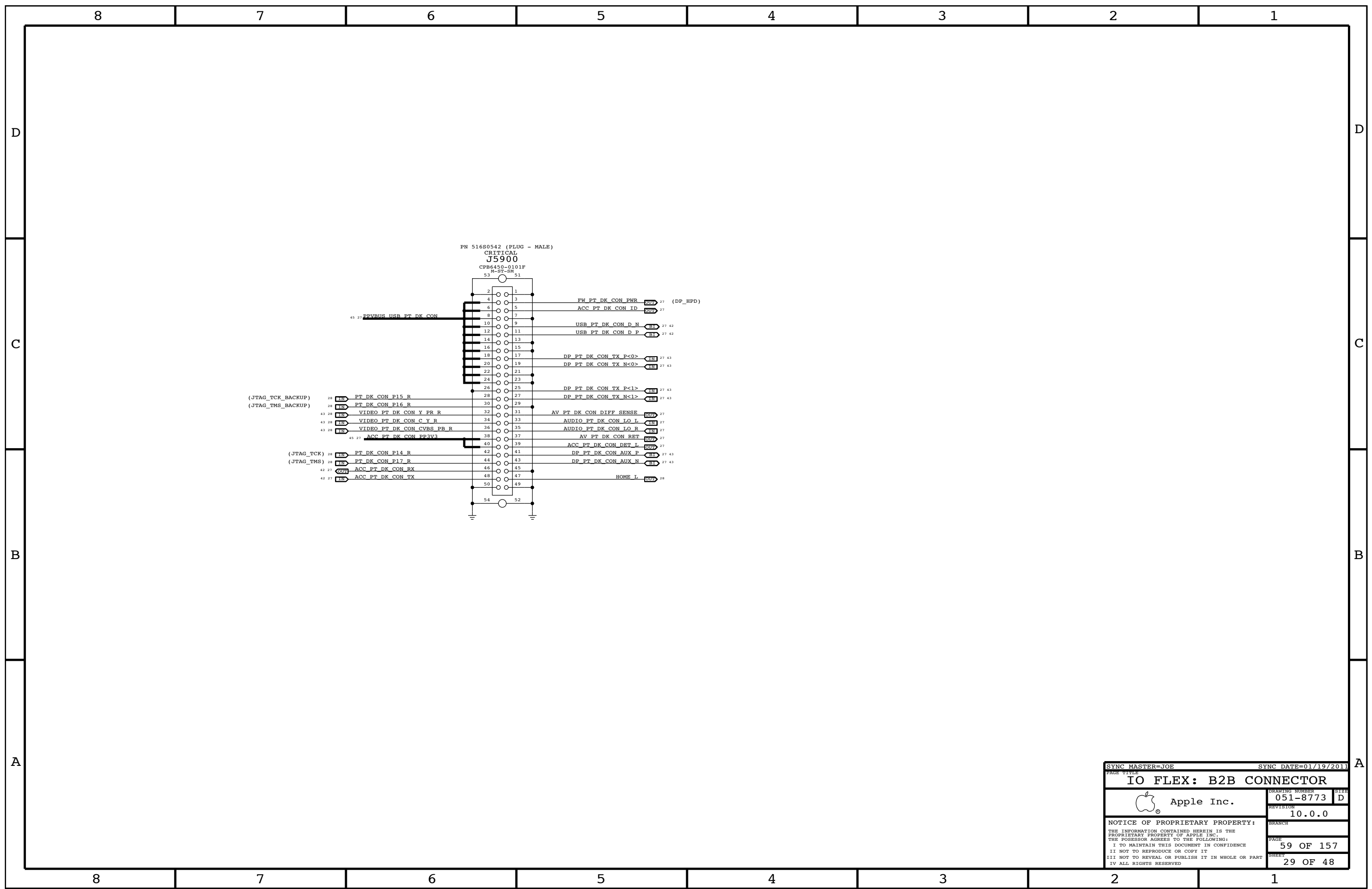
STUFFING OPTIONS FOR DP LANES 2, 3 FOR STEVENOTE.




FOR STEVENOTE ON MLB, STUFF ALL OF THE SNOTE BOM OPTIONS. NOSTUFF R5902, R5900, R5908 R5904, R5906, R5914, R5915, R5916, AND R5917. FOR DEV BOARD, STUFF R5918 AND NOSTUFF R5903.

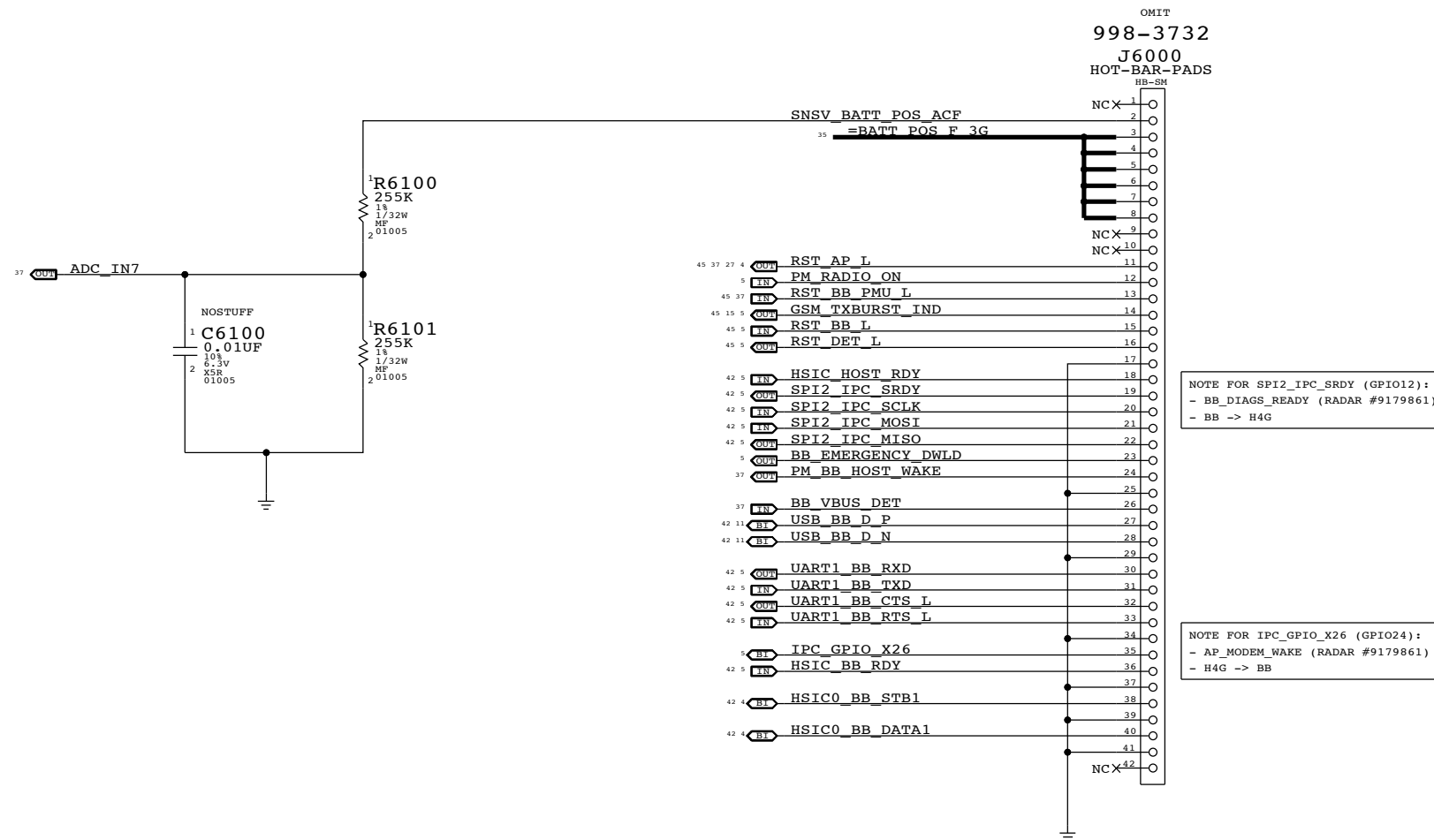


PAGE TITLE		SYNC MASTER=JOE		SYNC DATE=01/19/2011	
DISPLAY PORT MISC			DRAWING NUMBER	051-8773	SIZE
Apple Inc.			REVISION	10.0.0	D
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PAGE TITLE		SYNC MASTER=JOE		SYNC DATE=01/19/2011	
IO FLEX: B2B CONNECTOR					
 Apple Inc.		DRAWING NUMBER		SIZE	
		051-8773		D	
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		10.0.0			
		PAGE		SHEET	
		59 OF 157		29 OF 48	

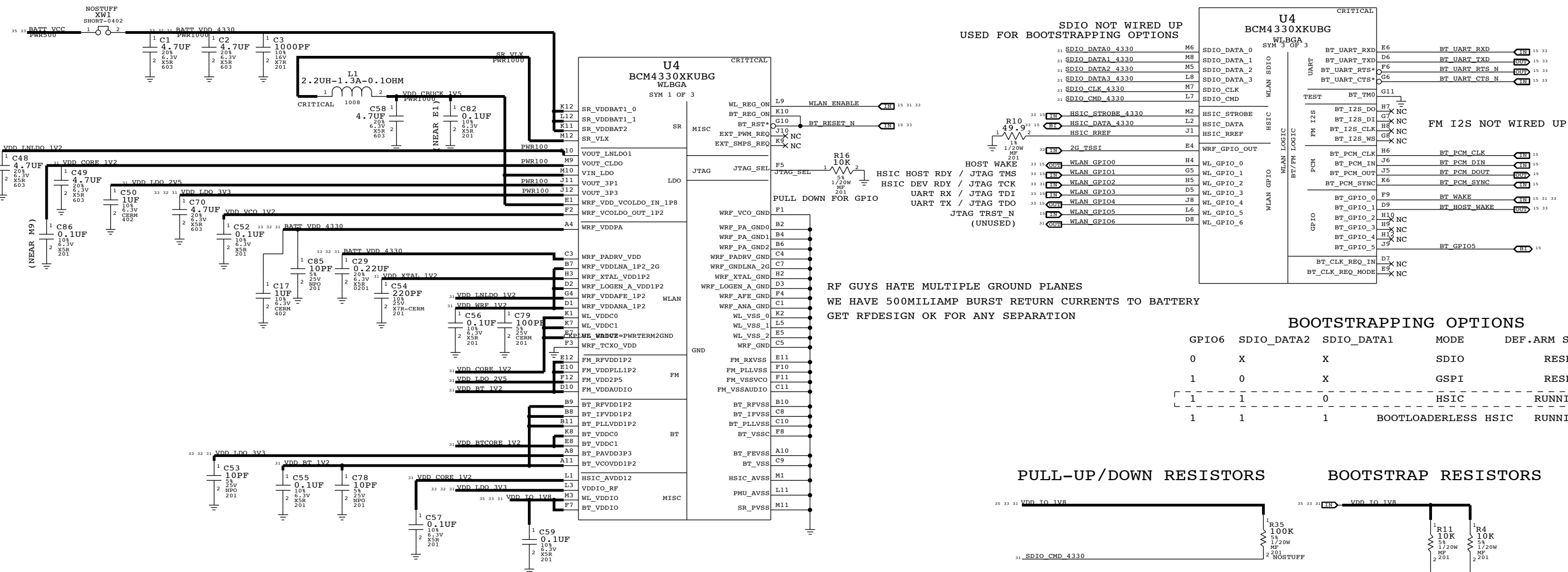
X26 CELLULAR/GPS CONNECTOR



SYNC MASTER=JOE		SYNC DATE=01/19/2011	
CONNECTOR: X26			
		DRAWING NUMBER	051-8773
		REVISION	10.0.0
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		PAGE	60 OF 157
		SHEET	30 OF 48
		SIZE	D

WLAN/BT POWER

WLAN/BT BASEBAND

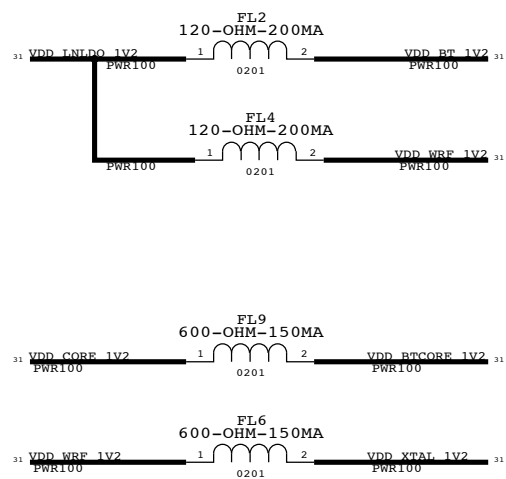


RF GUYS HATE MULTIPLE GROUND PLANES
WE HAVE 500MILIAMP BURST RETURN CURRENTS TO BATTERY
GET RFDESIGN OK FOR ANY SEPARATION

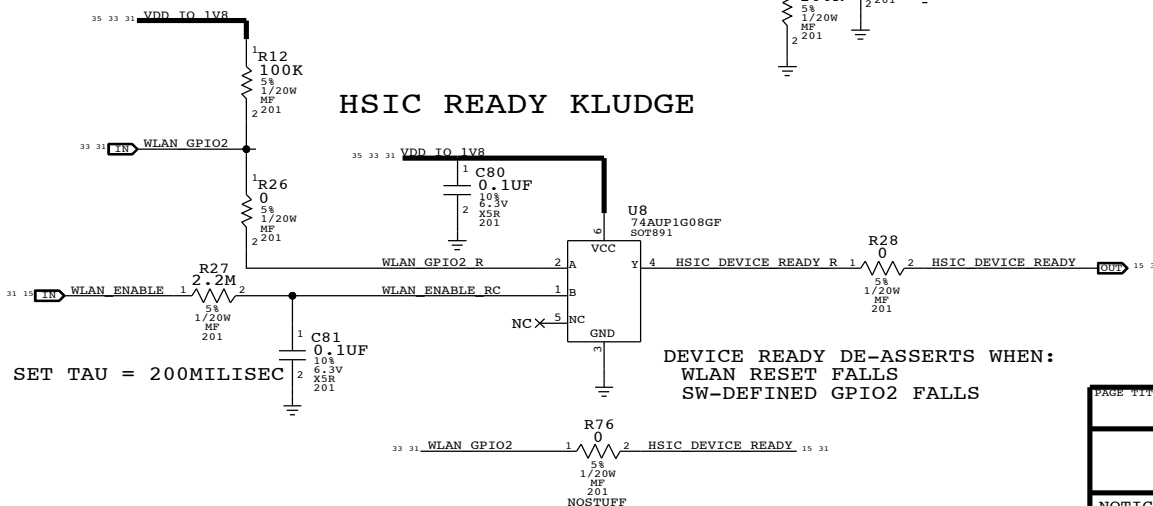
ALTERNATE PARTS AVAILABLE:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31180548	31180398	ANDGATE_TI	U8	TI
15580657	15580537	FERRITE_TY	FL2,FL4	TAIYO YUDEN
15580337	15580444	FERRITE_TDK	FL6,FL9	TDK

SUPPLY FILTERING



HSIC READY KLUDGE

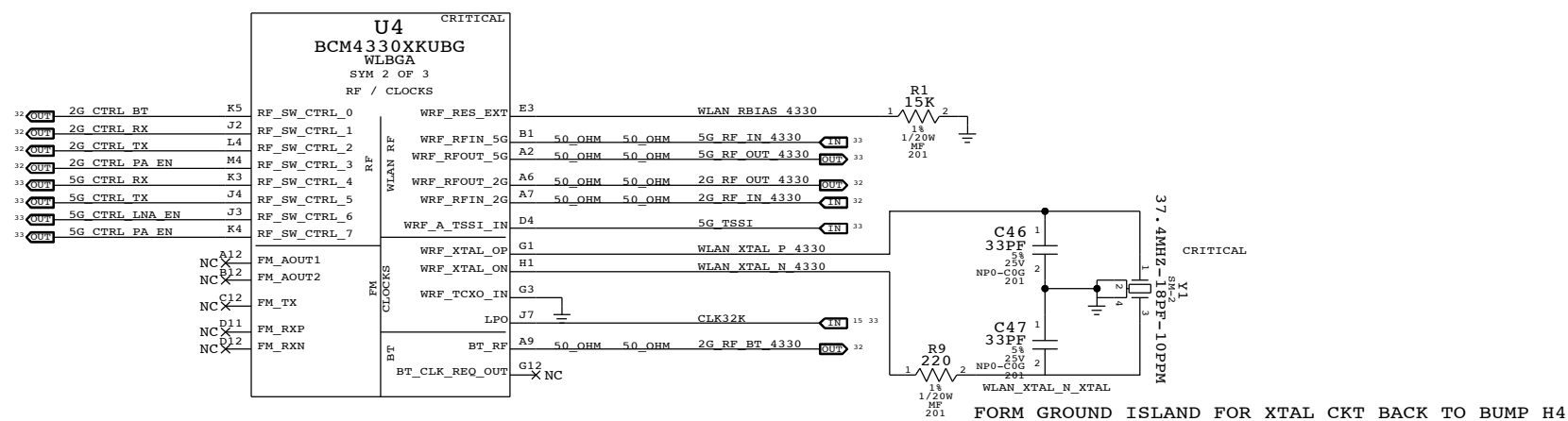


PAGE TITLE		DRAWING NUMBER	
WLAN BB & POWER		051-8773	SIZE D
Apple Inc.		REVISION 10.0.0	
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RF I/O PLAN

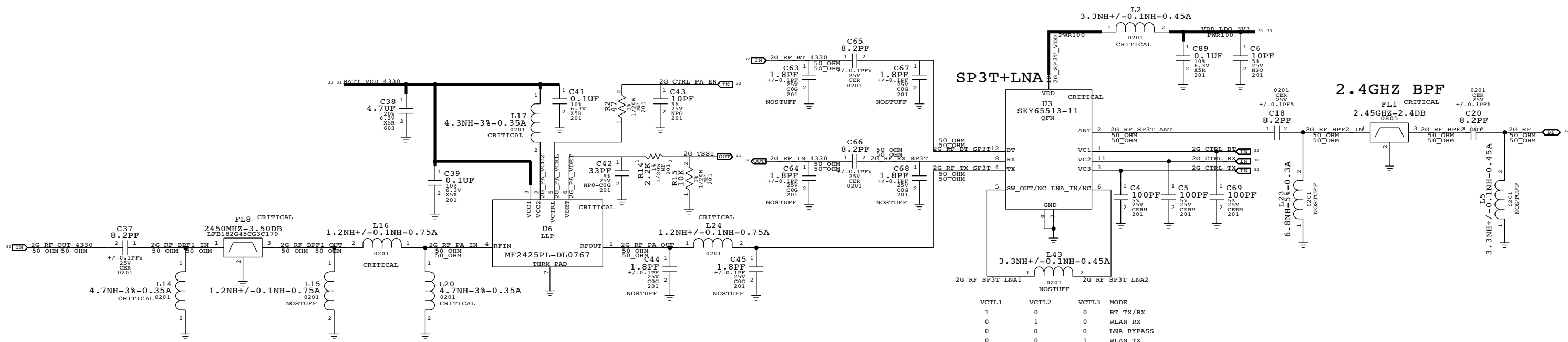
RF_SW_CTRL_0: 2G_CTRL_BT
 RF_SW_CTRL_1: 2G_CTRL_RX
 RF_SW_CTRL_2: 2G_CTRL_TX
 RF_SW_CTRL_3: 2G_CTRL_PA_EN
 RF_SW_CTRL_4: 5G_CTRL_RX
 RF_SW_CTRL_5: 5G_CTRL_TX
 RF_SW_CTRL_6: 5G_CTRL_LNA_EN
 RF_SW_CTRL_7: 5G_CTRL_PA_EN

WLAN TRANSCEIVER



2.4GHZ TX

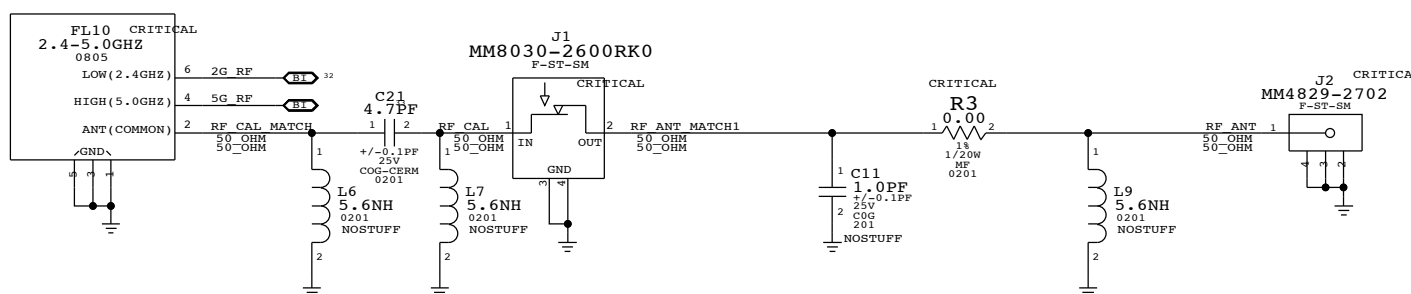
2.4GHZ RX + T/R SWITCH



2.4GHZ/5GHZ DIPLEXER

CONDUCTED TEST PORT

ANTENNA CONNECTOR

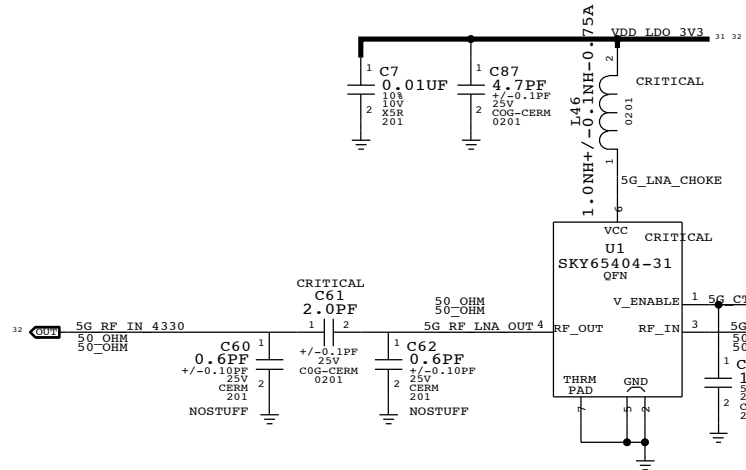


PAGE TITLE WLAN 2.4GHZ AND ANT		
Apple Inc.		DRAWING NUMBER 051-8773
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SHEET 32 OF 48		

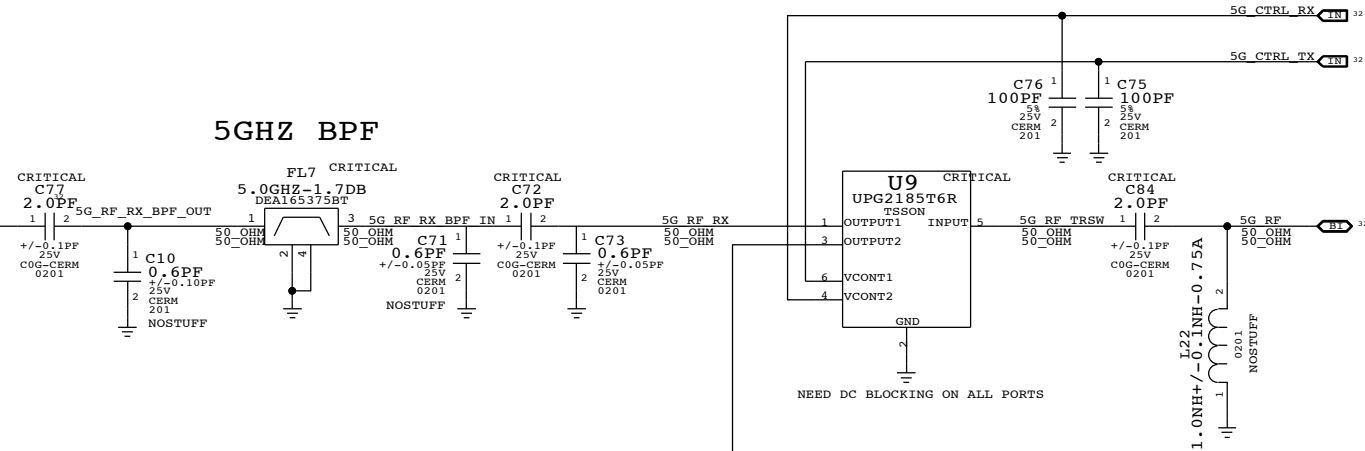
5GHZ FRONT-END CONTROL

VCRL1	VCTL2	PA_EN	LNA_EN	MODE
1	0	0	1	RX SUPERBYPASS MODE -- 26DB GAIN STEP
0	1	0	1	RX
1	0	1	0	TX

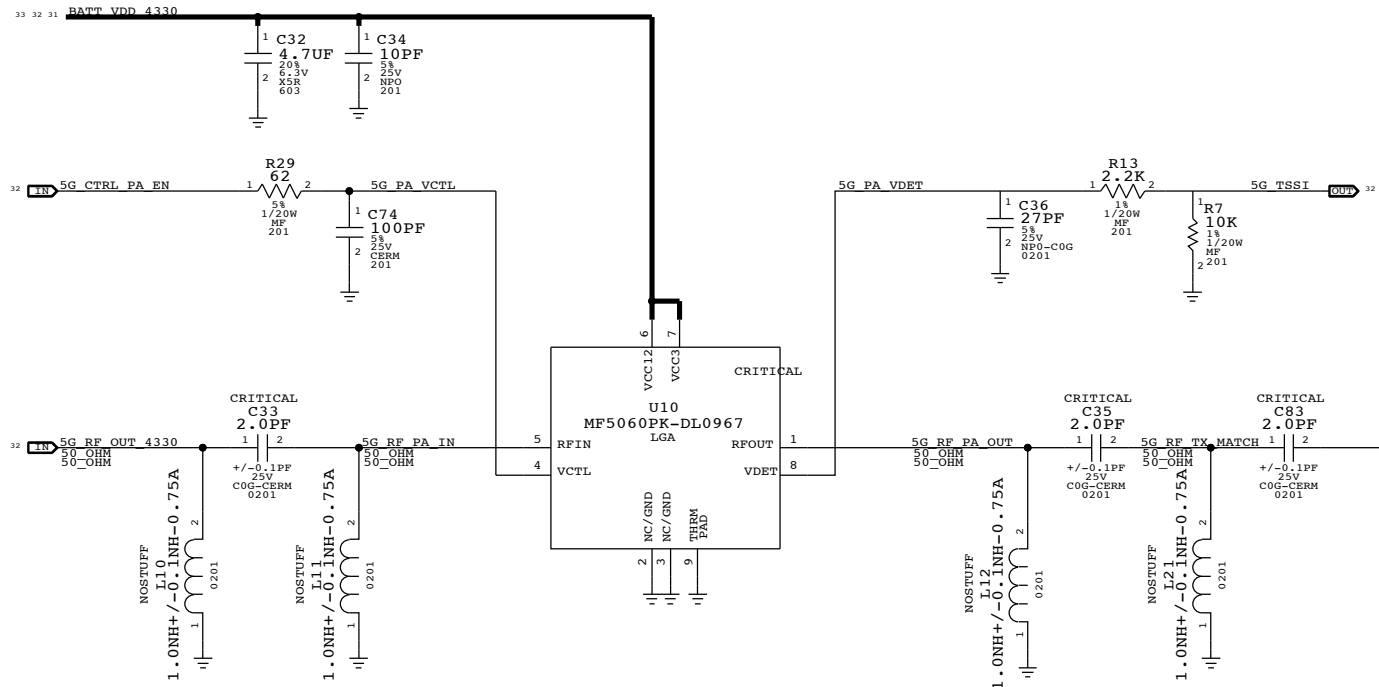
5GHZ LNA



5GHZ T/R SWITCH



5GHZ PA



TEST POINTS

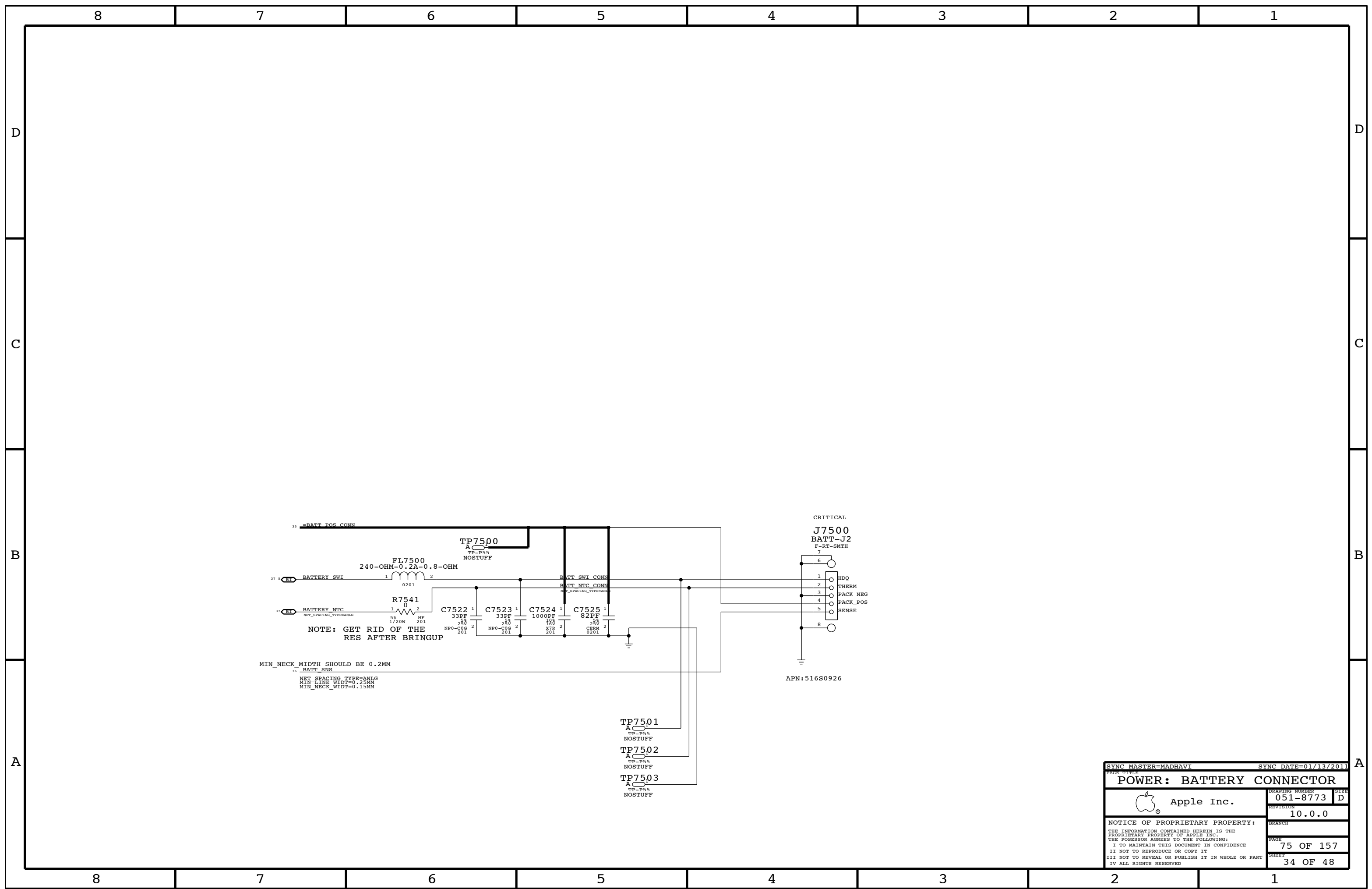
TEST AND PROBE POINTS

TP1 WLAN ENABLE	TP21 BT RESET N	TP15 BATT VCC
TP-P6 NOSTUFF	TP-P6 NOSTUFF	TP-1F0-TOP NOSTUFF
TP7 WLAN GPIO0	TP-P6 BT UART TXD	TP16 BATT VDD 4330
TP-P6 NOSTUFF	TP-P6 NOSTUFF	TP-1F0-TOP NOSTUFF
TP3 WLAN GPIO1	TP27 BT UART RXD	TP17 VDD IO 1V8
TP-P6 NOSTUFF	TP-P6 NOSTUFF	TP-1F0-TOP NOSTUFF
TP4 WLAN GPIO2	TP28 BT UART RTS N	TP18 NOSTUFF
TP-P6 NOSTUFF	TP-P6 NOSTUFF	TP-1F0-TOP NOSTUFF
TP5 WLAN GPIO3	TP29 BT UART CTS N	TP19 NOSTUFF
TP-P6 NOSTUFF	TP-P6 NOSTUFF	TP-1F0-TOP NOSTUFF
TP10 WLAN GPIO4	TP8 BT HOST WAKE	TP20 NOSTUFF
TP-P6 NOSTUFF	TP-P6 NOSTUFF	TP-1F0-TOP NOSTUFF
TP61 CLK32K	TP9 BT WAKE	TP-P6 NOSTUFF
TP-P6 NOSTUFF	TP-P6 NOSTUFF	

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WLAN 5GHZ AND TEST POINTS		051-8773	D
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PP29
F4MM
S1 1 HSIK DATA 4330 15 31

PP30
F4MM
S1 1 HSIK STROBE 4330 15 31



PAGE TITLE		SYNC MASTER=MADHAVI		SYNC DATE=01/13/2011	
POWER: BATTERY CONNECTOR					
Apple Inc.		DRAWING NUMBER	051-8773	SIZE	D
		REVISION	10.0.0	BRANCH	
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		PAGE	75 OF 157	SHEET	
				34 OF 48	

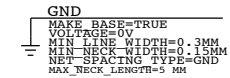
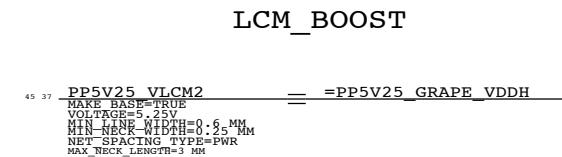
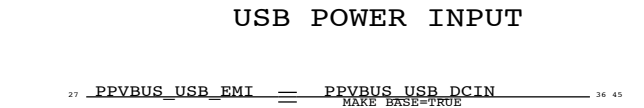
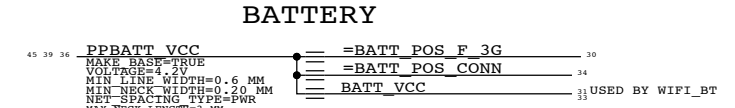
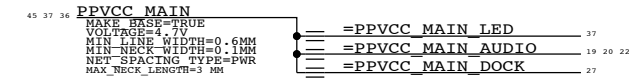
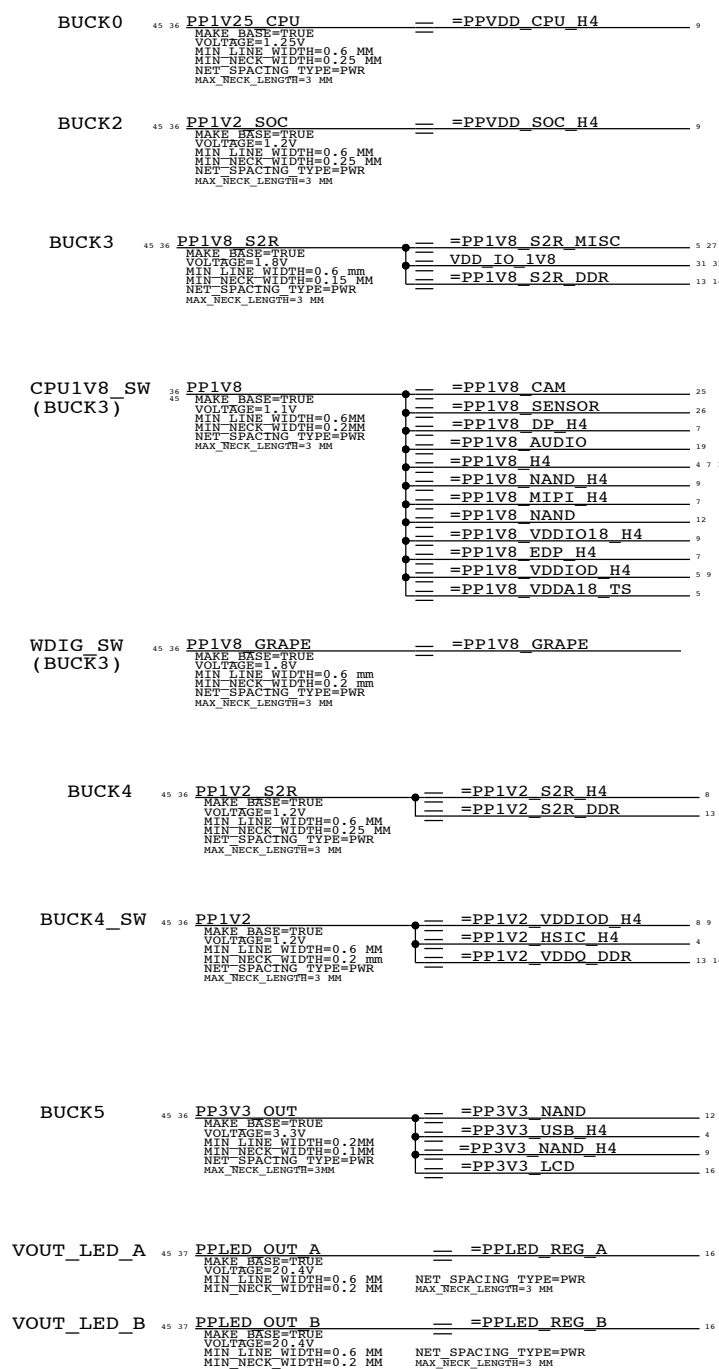
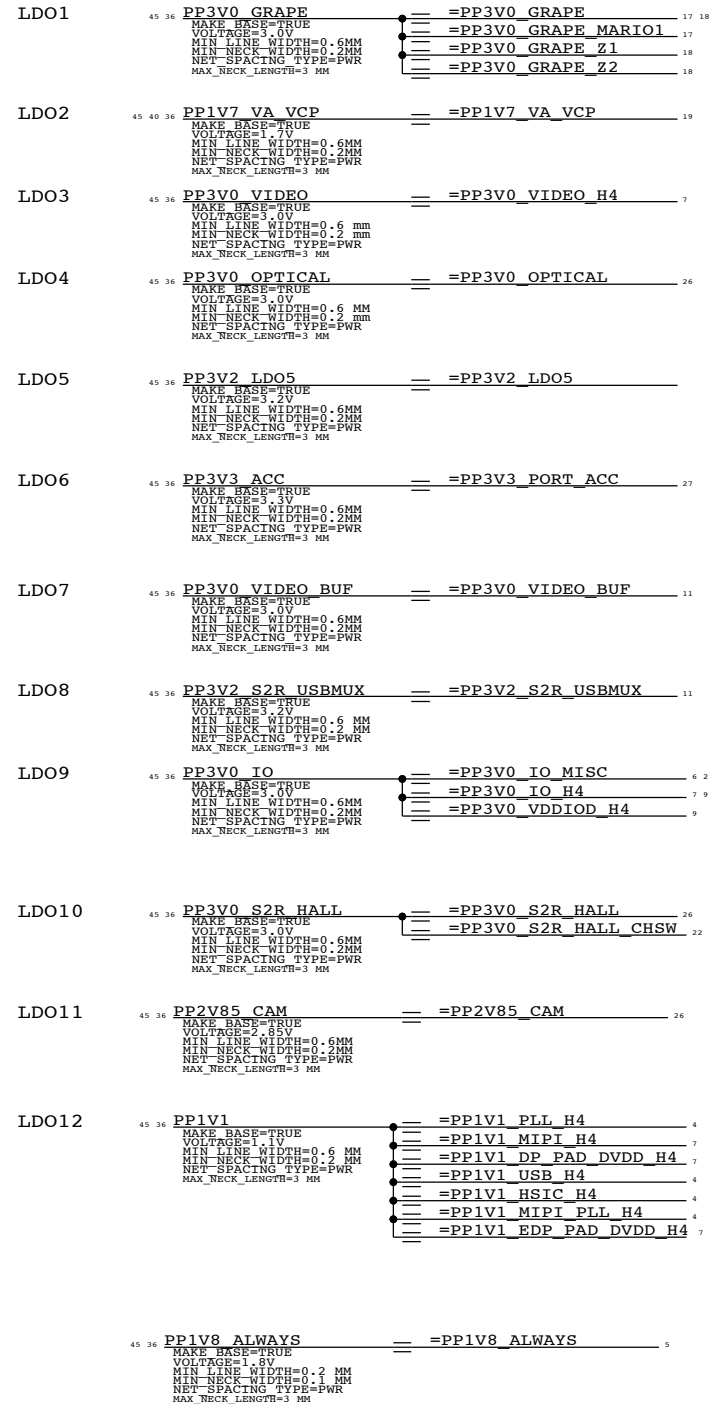
POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

BUCK RAILS

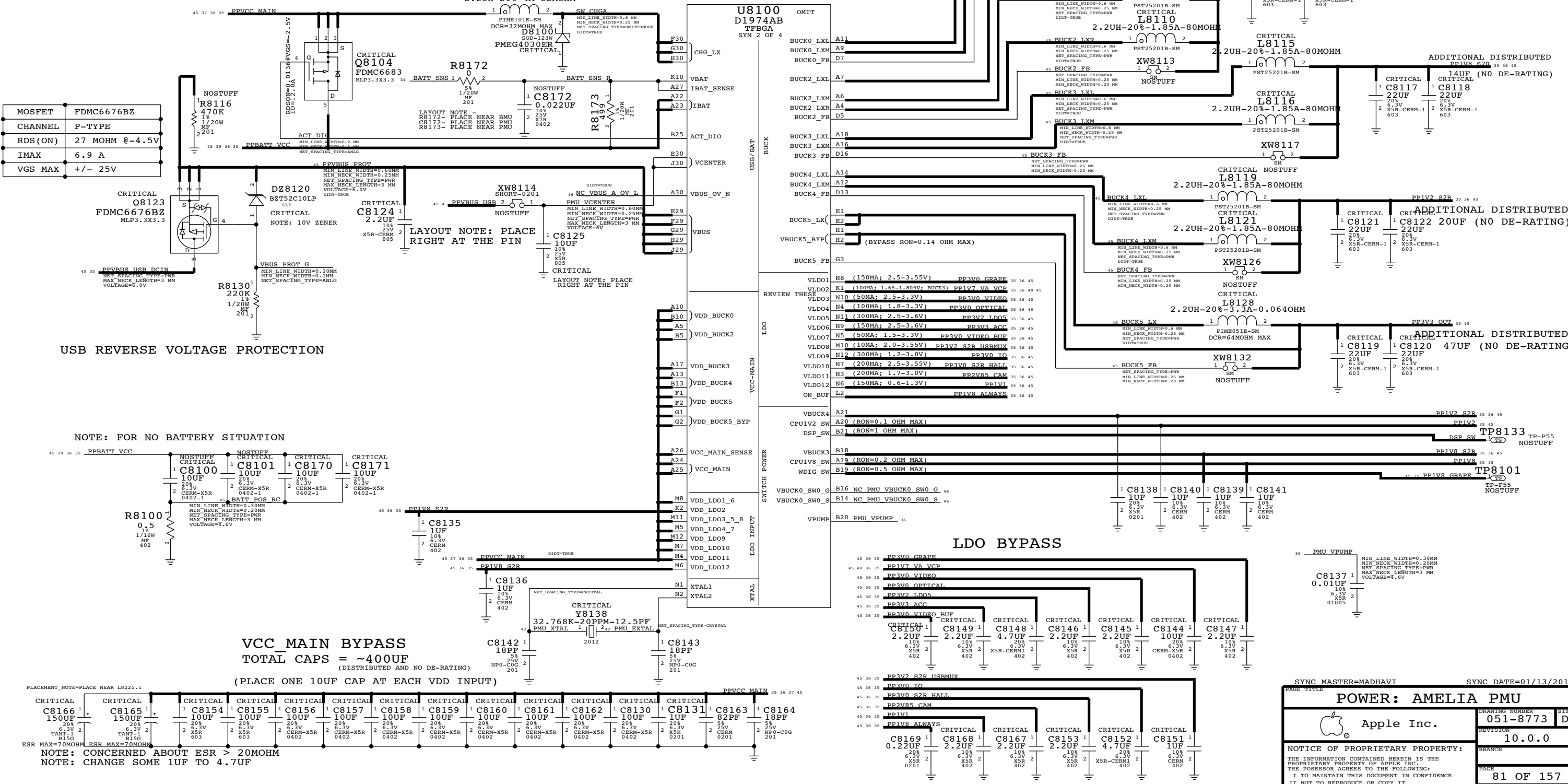
CHARGER MAIN



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POWER ALIASES					
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780392	19780299	?	Y8138	RADAR:8788152
15281452	15281292	?	L8128	RADAR:8376462

ALTERNATE FOUNDRY



PAGE TITLE: POWER: AMELIA PMU

Apple Inc.

DRAWING NUMBER: 051-8773

REVISION: 10.0.0

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SHEET: 36 OF 48

8 7 6 5 4 3 2 1

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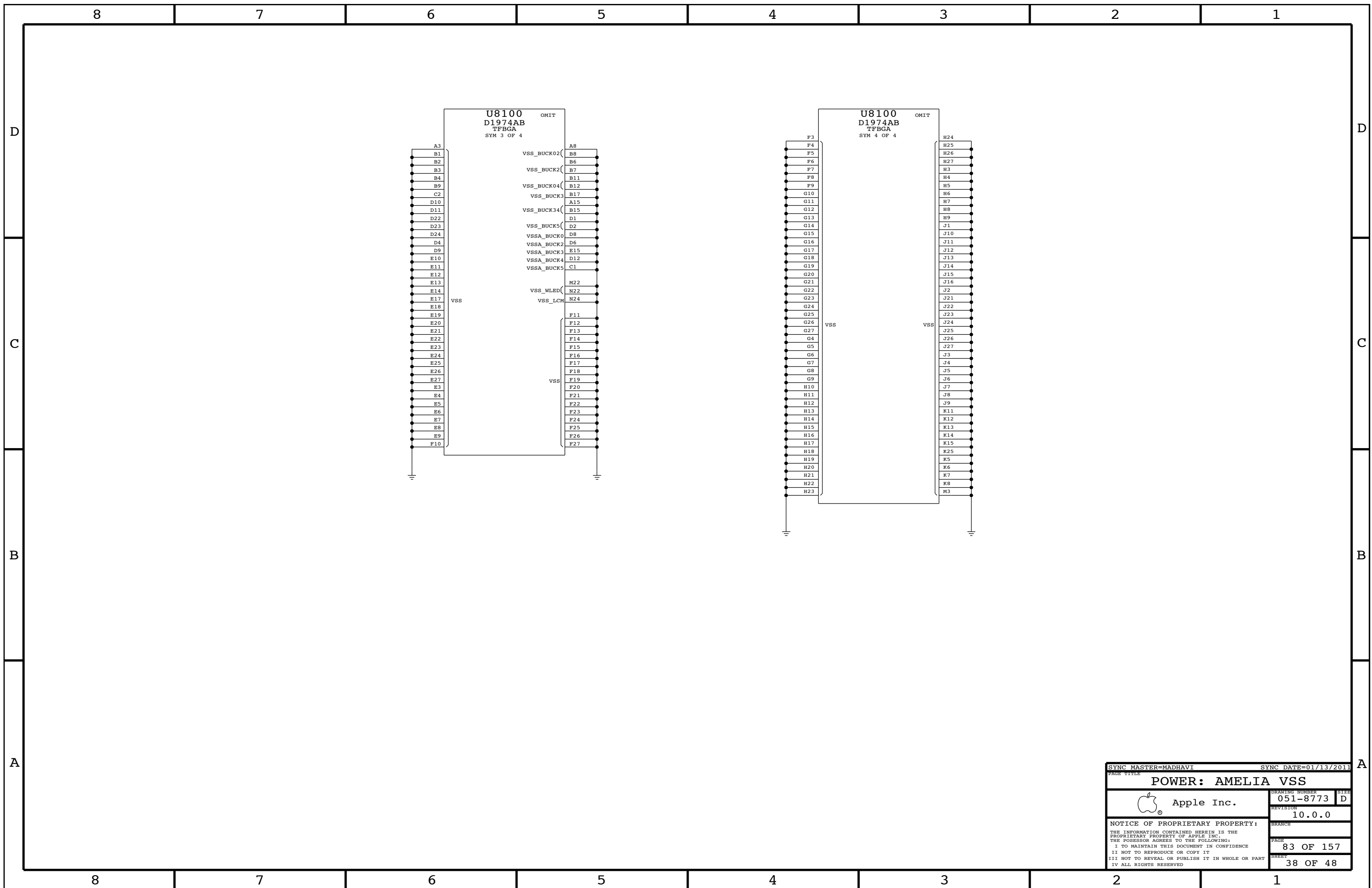
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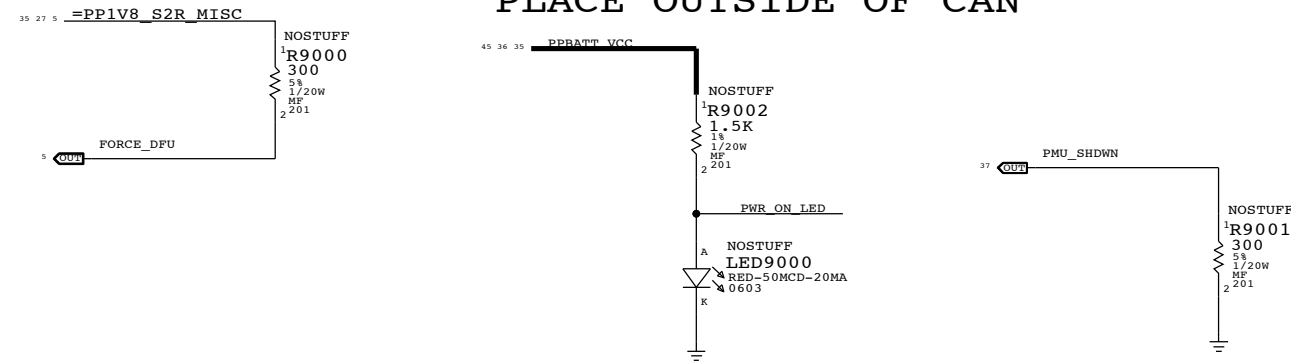
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		PAGE	83 OF 157
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DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN



SYNC MASTER=ALEX		SYNC DATE=10/04/2010	
PAGE TITLE DEBUG AND MISC			
		DRAWING NUMBER 051-8773	SIZE D
		REVISION 10.0.0	
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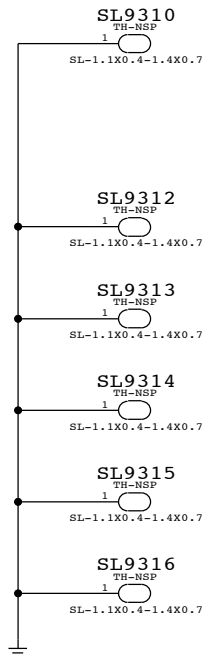
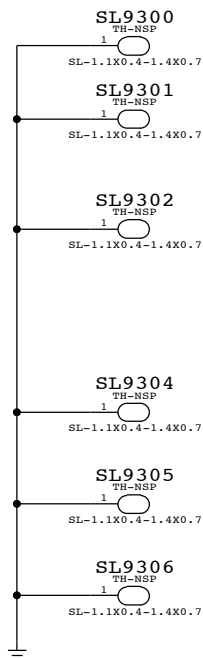
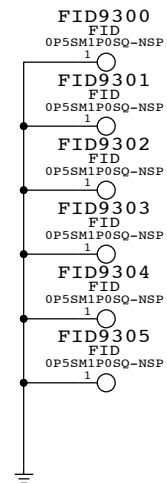
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PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



PROBE POINTS

- PP0
P4MM
SK
1 CODEC_LINE_OUT_REF 19 21
- PP1
P4MM
SK
1 CODEC_LINE_OUT_R 19 21
- PP2
P4MM
SK
1 AUD_SPKR_AMP2_PBUS 20
- PP3
P4MM
SK
1 AUD_SPKR_AMP1_PBUS 20
- PP4
P4MM
SK
1 CODEC_LINE_OUT_L 19 21
- PP5
P4MM
SK
1 DDR0_DQS_P<0> 8 13 44
- PP6
P4MM
SK
1 DDR0_DQ<0> 8 13 44
- PP7
P4MM
SK
1 DDR0_DQS_N<0> 8 13 44
- PP8
P4MM
SK
1 DDR0_DQS_N<1> 8 13 44
- PP9
P4MM
SK
1 DDR0_DQ<14> 8 13 44
- PP10
P4MM
SK
1 HSI_C1_WLAN_DATA1 4 15 42
- PP11
P4MM
SK
1 HSI_C1_WLAN_STB1 4 15 42
- PP12
P4MM
SK
1 Z1_BON_L<5> 17 18
- PP13
P4MM
SK
1 Z1_B_ADR<2> 17 18
- PP14
P4MM
SK
1 Z1_B_ADR<1> 17 18
- PP15
P4MM
SK
1 Z1_B_ADR<0> 17 18
- PP16
P4MM
SK
1 Z1_MISO 17 18
- PP17
P4MM
SK
1 Z1_BON_L<4> 17 18
- PP18
P4MM
SK
1 PP1V7_VA_VCP 35 36 45
- PP19
P4MM
SK
1 CONN_AUD_HEADSET_CHS_RET2 23 24
- PP20
P4MM
SK
1 CONN_AUD_HEADSET_CHS_MIC2 23 24
- PP21
P4MM
SK
1 CONN_AUD_HEADSET_DET 23 24
- PP22
P4MM
SK
1 AUD_HP1_DET_H 23
- PP23
P4MM
SK
1 AUD_HS_MIC2_RET 22 23
- PP24
P4MM
SK
1 AUD_HS_MIC1_HI 22 23
- PP25
P4MM
SK
1 AUD_HS_MIC1_RET 22 23
- PP26
P4MM
SK
1 AUD_HS_MIC2_HI 22 23

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SYNC MASTER=ALEX		SYNC DATE=10/04/2010	
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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA, BGA06-06	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES

45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL1, ISL12	Y	0.110 MM	0.060 MM	3.0 MM		
45_OHM_SE	ISL5, ISL8	Y	0.077 MM	0.060 MM	3.0 MM		
45_OHM_SE	ISL3	Y	0.055 MM	0.050 MM	3.0 MM		
45_OHM_SE	*	N	0.055 MM	0.050 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL1, ISL12	Y	0.088 MM	0.050 MM	3.0 MM		
50_OHM_SE	ISL3	Y	0.050 MM	0.050 MM	3.0 MM		
50_OHM_SE	ISL5, ISL8	Y	0.062 MM	0.050 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.110 MM	0.110 MM
90_OHM_DIFF	ISL3	Y	0.051 MM	0.051 MM	=STANDARD	0.120 MM	0.120 MM
90_OHM_DIFF	ISL5, ISL8	Y	0.072 MM	0.075 MM	=STANDARD	0.120 MM	0.120 MM

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM
LED	*	Y	0.2 MM	0.10MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.057 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.086 MM	?
2:1_SPACING	*	0.114 MM	?
2.5:1_SPACING	*	0.143 MM	?
3:1_SPACING	*	0.171 MM	?
4:1_SPACING	*	0.228 MM	?
5:1_SPACING	*	0.285 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP, BOTTOM	0.2 MM	1000

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.25 MM	10.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	10.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
LED	*	*	3:1_SPACING

NOTES:

- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

SYNC MASTER=MIKE		SYNC DATE=01/21/2011	
PAGE TITLE			
CONSTRAINTS: MLB RULES			
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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H100	CLK_50S	CLK	CLK 32K PMU 18 37
H101	CLK_50S	CLK	CLK 32K WLAN 19 37
H102	CLK_50S	CLK	CLK 32K GPS 19 37
H103	CLK_50S	CLK	CLK CAM_FF 7 25
H104	CLK_50S	CLK	CLK CAM_FF_FILT 25
H105	SE_50S	0P2MM_SPACING	CLK CAM_FF_CONN 24 25
H106	CLK_50S	CLK	CLK CAM_RF 7 25
H107	CLK_50S	CLK	CLK CAM_RF_FILT 25
H108	CLK_50S	CLK	CLK CAM_RF_CONN 24 25
H109	CLK_50S	CLK	I2S0 ASP MCK 5
H110	CLK_50S	CLK	I2S0 ASP MCK R 5 19
H111	CLK_50S	CLK	CLK CAM_FF_R 7
H112	CLK_50S	CLK	CLK CAM_FF_C 25
H113	CLK_50S	CLK	CLK CAM_FF_C 25

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H114	UART_50S	UART	UART0 AP_RXD 5 15
H115	UART_50S	UART	UART0 AP_TXD 5 15
H116	UART_50S	UART	UART0 MUX_RXD 11 15
H117	UART_50S	UART	UART0 MUX_TXD 11 15
H118	UART_50S	UART	UART1 BB_CTS_L 5 30
H119	UART_50S	UART	UART1 BB_RTS_L 5 30
H120	UART_50S	UART	UART1 BB_TXD 5 30
H121	UART_50S	UART	UART1 BB_RXD 5 30
H122	UART_50S	UART	UART3 BT_CTS_L 5 15
H123	UART_50S	UART	UART3 BT_RTS_L 5 15
H124	UART_50S	UART	UART3 BT_RXD 5 15
H125	UART_50S	UART	UART3 BT_TXD 5 15
H126	UART_50S	UART	UART6 WLAN_RXD 5 15
H127	UART_50S	UART	UART6 WLAN_TXD 5 15

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H128	SPI_50S	SPT	SPI1 GRAPE MISO 5 17
H129	SPI_50S	SPT	SPI1 GRAPE MOSI 5 17
H130	SPI_50S	SPT	SPI1 GRAPE SCLK 5 17
H131	SPI_50S	SPT	SPI1 GRAPE CS_L 5 17
H132	SPI_50S	SPT	SPI2 IPC MISO 5 30
H133	SPI_50S	SPT	SPI2 IPC MOSI 5 30
H134	SPI_50S	SPT	SPI2 IPC SCLK 5 30
H135	SPI_50S	SPT	SPI2 IPC SRDY 5 30

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H136		DWI	DWI AP_CLK 5 37
H137		DWI	DWI AP_DI 5 37
H138		DWI	DWI AP_DO 5 37

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H139		JTAG	JTAG AP_TCK 4 27
H140		JTAG	JTAG AP_TMS 4 27
H141		JTAG	JTAG AP_TDI 4 10
H142		JTAG	JTAG AP_TDO 4 10
H143		RST	JTAG AP_TRST_L 4 10 45

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H144	I2C_50S	I2C	I2C1_SDA_1V8 5 10 25
H145	I2C_50S	I2C	I2C1_SCL_1V8 5 10 25
H146	I2C_50S	I2C	I2C0_SDA_1V8 5 10 19 22 37
H147	I2C_50S	I2C	I2C0_SCL_1V8 5 10 19 22 37
H148	I2C_50S	I2C	I2C2_SDA_3V0 5 25
H149	I2C_50S	I2C	I2C2_SCL_3V0 5 25
H150	I2C_50S	I2C	ISP_AP_0_SCL 7 25
H151	I2C_50S	I2C	ISP_AP_0_SDA 7 25
H152	I2C_50S	I2C	ISP_AP_1_SCL 7 25
H153	I2C_50S	I2C	ISP_AP_1_SDA 7 25
H154	I2C_50S	I2C	I2C2_SCL_3V0_ALS 10 24 25
H155	I2C_50S	I2C	I2C2_SDA_3V0_ALS 10 24 25
H156	I2C_50S	I2C	I2C1_SCL_1V8_CONN 24 25
H157	I2C_50S	I2C	I2C1_SDA_1V8_CONN 24 25
H158	I2C_50S	I2C	ISP_CAM_1_SCL 24 25
H159	I2C_50S	I2C	ISP_CAM_1_SDA 24 25
H160	I2C_50S	I2C	ISP_CAM_0_SCL 24 25
H161	I2C_50S	I2C	ISP_CAM_0_SDA 24 25

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H162		CRYSTAL	XTAL_24M_I 4
H163		CRYSTAL	XTAL_24M_O 4
H164		CRYSTAL	24M_O 4
H165		CRYSTAL	PMU_XTAL 36
H166		CRYSTAL	PMU_EXTAL 36

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H167	I2S_90S	I2S	I2S0 ASP_BCLK 5 19
H168	I2S_90S	I2S	I2S0 ASP_LRCK 5 19
H169	I2S_90S	I2S	I2S0 ASP_DIN 5 19
H170	I2S_90S	I2S	I2S0 ASP_DOUT 5 19
H171	I2S_90S	I2S	I2S L63 ASP_SDOUT 19
H172	I2S_90S	I2S	I2S2 VSP_BCLK 5 15 19
H173	I2S_90S	I2S	I2S2 VSP_LRCK 5 15 19
H174	I2S_90S	I2S	I2S2 VSP_DIN 5 15 19
H175	I2S_90S	I2S	I2S2 VSP_DOUT 5 15 19
H176	I2S_90S	I2S	I2S L63 VSP_SDOUT 19
H177	I2S_90S	I2S	I2S3 XSP_BCLK 5 19
H178	I2S_90S	I2S	I2S3 XSP_LRCK 5 19
H179	I2S_90S	I2S	I2S3 XSP_DIN 5 19
H180	I2S_90S	I2S	I2S3 XSP_DOUT 5 19
H181	I2S_90S	I2S	I2S L63 XSP_SDOUT 19

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H182	USB_90D	USB	USB_DK_DO_P 4 27
H183	USB_90D	USB	USB_DK_DO_N 4 27
H184	USB_90D	USB	USB_DK_CON_DO_P 4 27
H185	USB_90D	USB	USB_DK_CON_DO_N 4 27
H186	USB_90D	USB	USB_BB_D_P 11 30
H187	USB_90D	USB	USB_BB_D_N 11 30
H188	USB_90D	USB	USB11_MUX_DO_P 4 11
H189	USB_90D	USB	USB11_MUX_DO_N 4 11
H190	USB_90D	USB	USB11_ACC_TX_N 11 27
H191	USB_90D	USB	USB11_ACC_RX_P 11 27
H192	USB_90D	USB	ACC_PT_DK_CON_TX 27 29
H193	USB_90D	USB	ACC_PT_DK_CON_RX 27 29
H194	USB_90D	USB	EXTRA_USB_D1_N
H195	USB_90D	USB	EXTRA_USB_D1_P
H196	USB_90D	USB	NC_USB11_D1_N 4 46
H197	USB_90D	USB	NC_USB11_D1_P 4 46
H198	USB_90D	USB	NC_USB_D1_N 4 46
H199	USB_90D	USB	NC_USB_D1_P 4 46
H200	USB_90D	USB	TP_WLAN_USB_DN
H201	USB_90D	USB	TP_WLAN_USB_DP
H202	USB_90D	USB	USB_GPIO_DM
H203	USB_90D	USB	USB_GPIO_DM_CONN
H204	USB_90D	USB	USB_GPIO_DP
H205	USB_90D	USB	USB_GPIO_DP_CONN
H206	USB_90D	USB	USB_PT_DK_CON_D_N 27 29
H207	USB_90D	USB	USB_PT_DK_CON_D_P 27 29
H208	USB_90D	USB	USB_UART_DM
H209	USB_90D	USB	USB_UART_DM_CONN
H210	USB_90D	USB	USB_UART_DP
H211	USB_90D	USB	USB_UART_DP_CONN
H212	USB_90D	USB	EXTRA_USB11_D1_N
H213	USB_90D	USB	EXTRA_USB11_D1_P

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
H214	HSIC	HSIC_BR	HSIC0_BB_DATA1 4 30
H215	HSIC	HSIC_BR	HSIC0_BB_STB1 4 30
H216	HSIC	HSIC_WLAN	HSIC1_WLAN_DATA1 4 15 40
H217	HSIC	HSIC_WLAN	HSIC1_WLAN_STB1 4 15 40
H218	HSIC	HSIC	HSIC_BB_RDY 5 30
H219	HSIC	HSIC	HSIC_HOST_RDY 5 30
H220	HSIC	HSIC	HSIC_HOST_READY_WL 5
H221	HSIC	HSIC	HSIC_HOST_READY_WLAN 5 15
H222	HSIC	HSIC	HSIC_WLAN_RDY 5 15
H223	HSIC	HSIC	NC_HSIC0_DATA2 4 46
H224	HSIC	HSIC	NC_HSIC0_STB2 4 46
H225	HSIC	HSIC	NC_HSIC1_DATA2 4 46
H226	HSIC	HSIC	NC_HSIC1_STB2 4 46

SYNC MASTER=MIKE SYNC DATE=01/21/2011

PAGE TITLE

CONSTRAINTS: LOW SPEED BUS

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	90_OHM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R220	DDR_50S	DDR	DDR0_CA<9..0> 4 13
R221	DDR_50S	DDR	DDR0_DM<3..0> 4 13
R222	DDR_90D	DDR	DDR0_CK_P 4 13
R223	DDR_90D	DDR	DDR0_CK_N 4 13
R224	DDR_50S	DDR	DDR0_CKE<1..0> 4 13
R225	DDR_50S	DDR	DDR0_CSN<2..0> 4 13
R226	DDR_50S	DDR	DDR0_ZQ 13
R227	DDR_50S	DDR0	DDR0_DQ<7..0> 4 13 40
R228	DDR_50S	DDR0	DDR0_DQS_P<0> 4 13 40
R229	DDR_50S	DDR0	DDR0_DQS_N<0> 4 13 40
R230	DDR_50S	DDR1	DDR0_DQ<15..8> 4 13 40
R231	DDR_50S	DDR1	DDR0_DQS_P<1> 4 13
R232	DDR_50S	DDR1	DDR0_DQS_N<1> 4 13 40
R233	DDR_50S	DDR2	DDR0_DQ<23..16> 4 13
R234	DDR_50S	DDR2	DDR0_DQS_P<2> 4 13
R235	DDR_50S	DDR2	DDR0_DQS_N<2> 4 13
R236	DDR_50S	DDR3	DDR0_DQ<31..24> 4 13
R237	DDR_50S	DDR3	DDR0_DQS_P<3> 4 13
R238	DDR_50S	DDR3	DDR0_DQS_N<3> 4 13
R239	DDR_50S	DDR	DDR1_CA<9..0> 4 13
R240	DDR_50S	DDR	DDR1_DM<3..0> 4 13
R241	DDR_90D	DDR	DDR1_CK_P 4 13
R242	DDR_90D	DDR	DDR1_CK_N 4 13
R243	DDR_50S	DDR	DDR1_CKE<1..0> 4 13
R244	DDR_50S	DDR	DDR1_CSN<2..0> 4 13
R245	DDR_50S	DDR	DDR1_ZQ 13
R246	DDR_50S	DDR0	DDR1_DQ<7..0> 4 13
R247	DDR_50S	DDR0	DDR1_DQS_P<0> 4 13
R248	DDR_50S	DDR0	DDR1_DQS_N<0> 4 13
R249	DDR_50S	DDR1	DDR1_DQ<15..8> 4 13
R250	DDR_50S	DDR1	DDR1_DQS_P<1> 4 13
R251	DDR_50S	DDR1	DDR1_DQS_N<1> 4 13
R252	DDR_50S	DDR2	DDR1_DQ<23..16> 4 13
R253	DDR_50S	DDR2	DDR1_DQS_P<2> 4 13
R254	DDR_50S	DDR2	DDR1_DQS_N<2> 4 13
R255	DDR_50S	DDR3	DDR1_DQ<31..24> 4 13
R256	DDR_50S	DDR3	DDR1_DQS_P<3> 4 13
R257	DDR_50S	DDR3	DDR1_DQS_N<3> 4 13
R258	DDR_50S	DDR	DDR2_CA<9..0> 4 14
R259	DDR_50S	DDR	DDR2_DM<3..0> 4 14
R260	DDR_90D	DDR	DDR2_CK_P 4 14
R261	DDR_90D	DDR	DDR2_CK_N 4 14
R262	DDR_50S	DDR	DDR2_CKE<1..0> 4 14
R263	DDR_50S	DDR	DDR2_CSN<2..0> 4 14
R264	DDR_50S	DDR	DDR2_ZQ 14
R265	DDR_50S	DDR0	DDR2_DQ<7..0> 4 14
R266	DDR_50S	DDR0	DDR2_DQS_P<0> 4 14
R267	DDR_50S	DDR0	DDR2_DQS_N<0> 4 14
R268	DDR_50S	DDR1	DDR2_DQ<15..8> 4 14
R269	DDR_50S	DDR1	DDR2_DQS_P<1> 4 14
R270	DDR_50S	DDR1	DDR2_DQS_N<1> 4 14
R271	DDR_50S	DDR2	DDR2_DQ<23..16> 4 14
R272	DDR_50S	DDR2	DDR2_DQS_P<2> 4 14
R273	DDR_50S	DDR2	DDR2_DQS_N<2> 4 14
R274	DDR_50S	DDR3	DDR2_DQ<31..24> 4 14
R275	DDR_50S	DDR3	DDR2_DQS_P<3> 4 14
R276	DDR_50S	DDR3	DDR2_DQS_N<3> 4 14
R277	DDR_50S	DDR	DDR3_CA<9..0> 4 14
R278	DDR_50S	DDR	DDR3_DM<3..0> 4 14
R279	DDR_90D	DDR	DDR3_CK_P 4 14
R280	DDR_90D	DDR	DDR3_CK_N 4 14
R281	DDR_50S	DDR	DDR3_CKE<1..0> 4 14
R282	DDR_50S	DDR	DDR3_CSN<2..0> 4 14
R283	DDR_50S	DDR	DDR3_ZQ 14
R284	DDR_50S	DDR0	DDR3_DQ<7..0> 4 14
R285	DDR_50S	DDR0	DDR3_DQS_P<0> 4 14
R286	DDR_50S	DDR0	DDR3_DQS_N<0> 4 14
R287	DDR_50S	DDR1	DDR3_DQ<15..8> 4 14
R288	DDR_50S	DDR1	DDR3_DQS_P<1> 4 14
R289	DDR_50S	DDR1	DDR3_DQS_N<1> 4 14
R290	DDR_50S	DDR2	DDR3_DQ<23..16> 4 14
R291	DDR_50S	DDR2	DDR3_DQS_P<2> 4 14
R292	DDR_50S	DDR2	DDR3_DQS_N<2> 4 14
R293	DDR_50S	DDR3	DDR3_DQ<31..24> 4 14
R294	DDR_50S	DDR3	DDR3_DQS_P<3> 4 14
R295	DDR_50S	DDR3	DDR3_DQS_N<3> 4 14

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R400	NAND_50S	NAND0	FMIO_AD<0> 4 12
R401	NAND_50S	NAND0	FMIO_AD<1> 4 12
R402	NAND_50S	NAND0	FMIO_AD<2> 4 12
R403	NAND_50S	NAND0	FMIO_AD<3> 4 12
R404	NAND_50S	NAND0	FMIO_AD<4> 4 12
R405	NAND_50S	NAND0	FMIO_AD<5> 4 12
R406	NAND_50S	NAND0	FMIO_AD<6> 4 12
R407	NAND_50S	NAND0	FMIO_AD<7> 4 12
R408	NAND_50S	NAND0	FMIO_ALE 4 12
R409	NAND_50S	NAND0	FMIO_CE0_L 4 12
R410	NAND_50S	NAND0	FMIO_CE1_L 4 12
R411	NAND_50S	NAND0	FMIO_CE2_L 4 12
R412	NAND_50S	NAND0	FMIO_CE3_L 4 12
R413	NAND_50S	NAND0	FMIO_CE4_L 4 12
R414	NAND_50S	NAND0	FMIO_CE5_L 4 12
R415	NAND_50S	NAND0	FMIO_CE6_L 4 12
R416	NAND_50S	NAND0	FMIO_CE7_L 4 12
R417	NAND_50S	NAND0	FMIO_CLE 4 12
R418	NAND_50S	NAND0	FMIO_DOS_N 4 12
R419	NAND_50S	NAND0	FMIO_DOS_P 4 12
R420	NAND_50S	NAND0	FMIO_RB0_L 4 12
R421	NAND_50S	NAND0	FMIO_RB1_L 4 12
R422	NAND_50S	NAND0	FMIO_RE_N 4 12
R423	NAND_50S	NAND0	FMIO_RE_P 4 12
R424	NAND_50S	NAND0	FMIO_WE_L 4 12
R425	NAND_50S	NAND0	FMIO_WP_L 4 12
R426	NAND_50S	NAND1	FM11_AD<0> 4 12
R427	NAND_50S	NAND1	FM11_AD<1> 4 12
R428	NAND_50S	NAND1	FM11_AD<2> 4 12
R429	NAND_50S	NAND1	FM11_AD<3> 4 12
R430	NAND_50S	NAND1	FM11_AD<4> 4 12
R431	NAND_50S	NAND1	FM11_AD<5> 4 12
R432	NAND_50S	NAND1	FM11_AD<6> 4 12
R433	NAND_50S	NAND1	FM11_AD<7> 4 12
R434	NAND_50S	NAND1	FM11_ALE 4 12 44
R435	NAND_50S	NAND1	FM11_CE0_L 4 12
R436	NAND_50S	NAND1	FM11_CE1_L 4 12
R437	NAND_50S	NAND1	FM11_CE2_L 4 12
R438	NAND_50S	NAND1	FM11_CE3_L 4 12
R439	NAND_50S	NAND1	FM11_CE4_L 4 12
R440	NAND_50S	NAND1	FM11_CE5_L 4 12
R441	NAND_50S	NAND1	FM11_CE6_L 4 12
R442	NAND_50S	NAND1	FM11_CE7_L 4 12
R443	NAND_50S	NAND1	FM11_CLE 4 12 44
R444	NAND_50S	NAND1	FM11_DOS_N 4 12
R445	NAND_50S	NAND1	FM11_DOS_P 4 12
R446	NAND_50S	NAND1	FM11_RB0_L 4 12
R447	NAND_50S	NAND1	FM11_RB1_L 4 12
R448	NAND_50S	NAND1	FM11_RE_N 4 12
R449	NAND_50S	NAND1	FM11_RE_P 4 12
R450	NAND_50S	NAND1	FM11_WE_L 4 12 44
R451	NAND_50S	NAND1	FM11_WP_L 4 12 44
R452	NAND_50S	NAND1	FM11_ALE 4 12 44
R453	NAND_50S	NAND1	FM11_RE_L 4 12 44
R454	NAND_50S	NAND1	FM11_WE_L 4 12 44
R455	NAND_50S	NAND1	FM11_WP_L 4 12 44

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R460	PWR	PWR	PPVREF_DDR0_CA 13 45
R461	PWR	PWR	PPVREF_DDR0_DQ 13 45
R462	PWR	PWR	PPVREF_DDR1_CA 13 45
R463	PWR	PWR	PPVREF_DDR1_DQ 13 45

NAND DEV

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
R470	NAND_50S	NAND0	SLOT0_FMIO_AD<0>
R471	NAND_50S	NAND0	SLOT0_FMIO_AD<1>
R472	NAND_50S	NAND0	SLOT0_FMIO_AD<2>
R473	NAND_50S	NAND0	SLOT0_FMIO_AD<3>
R474	NAND_50S	NAND0	SLOT0_FMIO_AD<4>
R475	NAND_50S	NAND0	SLOT0_FMIO_AD<5>
R476	NAND_50S	NAND0	SLOT0_FMIO_AD<6>
R477	NAND_50S	NAND0	SLOT0_FMIO_AD<7>
R478	NAND_50S	NAND0	SLOT0_FMIO_ALE
R479	NAND_50S	NAND0	SLOT0_FMIO_CE0_L
R480	NAND_50S	NAND0	SLOT0_FMIO_CE1_L
R481	NAND_50S	NAND0	SLOT0_FMIO_CLE
R482	NAND_50S	NAND0	SLOT0_FMIO_DQS_P
R483	NAND_50S	NAND0	SLOT0_FMIO_RE_N
R484	NAND_50S	NAND0	SLOT0_FMIO_WE_L
R485	NAND_50S	NAND1	SLOT0_FM11_AD<0>
R486	NAND_50S	NAND1	SLOT0_FM11_AD<1>
R487	NAND_50S	NAND1	SLOT0_FM11_AD<2>
R488	NAND_50S	NAND1	SLOT0_FM11_AD<3>
R489	NAND_50S	NAND1	SLOT0_FM11_AD<4>
R490	NAND_50S	NAND1	SLOT0_FM11_AD<5>
R491	NAND_50S	NAND1	SLOT0_FM11_AD<6>
R492	NAND_50S	NAND1	SLOT0_FM11_AD<7>
R493	NAND_50S	NAND1	SLOT0_FM11_ALE
R494	NAND_50S	NAND1	SLOT0_FM11_CE0_L
R495	NAND_50S	NAND1	SLOT0_FM11_CE1_L
R496	NAND_50S	NAND1	SLOT0_FM11_CLE
R497	NAND_50S	NAND1	SLOT0_FM11_DQS_P
R498	NAND_50S	NAND1	SLOT0_FM11_RE_N
R499	NAND_50S	NAND1	SLOT0_FM11_WE_L
R500	NAND_50S	NAND0	SLOT1_FMIO_AD<0>
R501	NAND_50S	NAND0	SLOT1_FMIO_AD<1>
R502	NAND_50S	NAND0	SLOT1_FMIO_AD<2>
R503	NAND_50S	NAND0	SLOT1_FMIO_AD<3>
R504	NAND_50S	NAND0	SLOT1_FMIO_AD<4>
R505	NAND_50S	NAND0	SLOT1_FMIO_AD<5>
R506	NAND_50S	NAND0	SLOT1_FMIO_AD<6>
R507	NAND_50S	NAND0	SLOT1_FMIO_AD<7>
R508	NAND_50S	NAND0	SLOT1_FMIO_ALE
R509	NAND_50S	NAND0	SLOT1_FMIO_CE0_L
R510	NAND_50S	NAND0	SLOT1_FMIO_CE1_L
R511	NAND_50S	NAND0	SLOT1_FMIO_CLE
R512	NAND_50S	NAND0	SLOT1_FMIO_DQS_P
R513	NAND_50S	NAND0	SLOT1_FMIO_RE_N
R514	NAND_50S	NAND0	SLOT1_FMIO_WE_L
R515	NAND_50S	NAND1	SLOT1_FM11_AD<0>
R516	NAND_50S	NAND1	SLOT1_FM11_AD<1>
R517	NAND_50S	NAND1	SLOT1_FM11_AD<2>
R518	NAND_50S	NAND1	SLOT1_FM11_AD<3>
R519	NAND_50S	NAND1	SLOT1_FM11_AD<4>
R520	NAND_50S	NAND1	SLOT1_FM11_AD<5>
R521	NAND_50S	NAND1	SLOT1_FM11_AD<6>
R522	NAND_50S	NAND1	SLOT1_FM11_AD<7>
R523	NAND_50S	NAND1	SLOT1_FM11_ALE
R524	NAND_50S	NAND1	SLOT1_FM11_CE0_L
R525	NAND_50S	NAND1	SLOT1_FM11_CE1_L
R526	NAND_50S	NAND1	SLOT1_FM11_CLE
R527	NAND_50S	NAND1	SLOT1_FM11_DQS_P
R528	NAND_50S	NAND1	SLOT1_FM11_RE_N
R529	NAND_50S	NAND1	SLOT1_FM11_WE_L

SYNC MASTER=MIKE SYNC DATE=01/21/2011

CONSTRAINTS: DDR/FMI

Apple Inc.

DRAWING NUMBER: 051-8773 SIZE: D

REVISION: 10.0.0

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PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H255	3.0V	PP_PWR	PWR	MT 3V3 INT 18 45
H256	1.8V	PP_PWR	PWR	Z1 1V8 OUT 18
H257	1.8V	PP_PWR	PWR	Z2 VDDCORE 18
H258	1.8V	PP_PWR	PWR	Z2 VDDANA 18
H259	1.8V	PP_PWR	PWR	Z2 3V3 1V8 IN 18

VOLTAGE	NET_TYPE			
	PHYSICAL	SPACING		
H229	3.3V	PP_PWR	PWR	ACC_PT_DK_CON_PP3V3 27 29
H230		PP_PWR	PWR	BUCK0_FB 36
H231		PP_PWR	PWR	BUCK0_LXL 36
H232		PP_PWR	PWR	BUCK0_LXM 36
H233		PP_PWR	PWR	BUCK2_FB 36
H234		PP_PWR	PWR	BUCK2_LXL 36
H235		PP_PWR	PWR	BUCK2_LXM 36
H236		PP_PWR	PWR	BUCK2_LXR 36
H237		PP_PWR	PWR	BUCK3_FB 36
H238		PP_PWR	PWR	BUCK3_LXL 36
H239		PP_PWR	PWR	BUCK3_LXM 36
H240		PP_PWR	PWR	BUCK4_FB 36
H241		PP_PWR	PWR	BUCK4_LXL 36
H242		PP_PWR	PWR	BUCK4_LXM 36
H243		PP_PWR	PWR	BUCK5_FB 36
H244		PP_PWR	PWR	BUCK5_LX 36
H245	0.4V	PP_PWR	PWR	PP0V4_MIPI0D 7
H246	0.4V	PP_PWR	PWR	PP0V4_MIPI1D 7
H247	1.1V	PP_PWR	PWR	PP1V1 35 36
H248	1.2V	PP_PWR	PWR	PP1V2 35 36
H249	1.1V	PP_PWR	PWR	PP1V8 35 36
H250	1.1V	PP_PWR	PWR	PP1V1_MIPID_PLL_F 4
H251	1.1V	PP_PWR	PWR	PP1V1_PL0_F 4
H252	1.1V	PP_PWR	PWR	PP1V1_PL1_F 4
H253	1.1V	PP_PWR	PWR	PP1V1_PL2_F 4
H254	1.1V	PP_PWR	PWR	PP1V1_PL3_F 4
H255	1.1V	PP_PWR	PWR	PP1V1_PL4_F 4
H256	1.1V	PP_PWR	PWR	PP1V1_PL5_F 4
H257	1.1V	PP_PWR	PWR	PP1V1_PLL_USB_F 4
H258	1.25V	PP_PWR	PWR	PP1V25_CPU 35 36
H259	1.2V	PP_PWR	PWR	PP1V2_S2R 35 36
H260	1.2V	PP_PWR	PWR	PP1V2_SOC 35 36
H261	1.2V	PP_PWR	PWR	PP1V7_VA_VCP 35 36 40
H262	1.8V	PP_PWR	PWR	PP1V8_ALWAYS 35 36
H263	1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX 7
H264	1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX 7
H265	1.8V	PP_PWR	PWR	PP1V8_GRAPE 35 36
H266	1.8V	PP_PWR	PWR	PP1V8_S2R 35 36
H267	1.8V	PP_PWR	PWR	PP1V8_SENSOR_FLT 24 26
H268	1.8V	PP_PWR	PWR	PP1V8_VDDA18_TS 5
H269	2.85V	PP_PWR	PWR	PP2V85_CAM 35 36
H270	2.85V	PP_PWR	PWR	PP2V85_CAM_FLT 24 26
H271	3.0V	PP_PWR	PWR	PP3V0_GRAPE 35 36
H272	3.0V	PP_PWR	PWR	PP3V0_IO 35 36
H273	3.0V	PP_PWR	PWR	PP3V0_OPTICAL 35 36
H274	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL 35 36
H275	3.0V	PP_PWR	PWR	PP3V0_S2R_HALL_FLT 24 26
H276	3.0V	PP_PWR	PWR	PP3V0_SENSOR_FLT 10 24 26
H277	3.0V	PP_PWR	PWR	PP3V0_VIDEO 35 36
H278	3.0V	PP_PWR	PWR	PP3V0_VIDEO_BUF 35 36
H279	3.2V	PP_PWR	PWR	PP3V2_LDO5 35 36
H280	3.2V	PP_PWR	PWR	PP3V2_S2R_USBMUX 35 36
H281	3.3V	PP_PWR	PWR	PP3V3_ACC 35 36
H282	3.3V	PP_PWR	PWR	PP3V3_LCDVDD_SW_F 16
H283	3.3V	PP_PWR	PWR	PP3V3_OUT 35 36
H284	3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR 16
H285	5.25V	PP_PWR	PWR	PP5V25_VLCM2 35 37
H286	6.0V	PP_PWR	PWR	PP6V0_LCM_HI 37
H287	6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST 37
H288	4.2V	PWR500	PWR	PPBATT_VCC 35 36 39
H289	1.8V	PP_PWR	PWR	PPIO_NAND_H4 6 9
H290	20.4V	PP_PWR	PWR	PPLED_BACK_REG_A 16
H291	20.4V	PP_PWR	PWR	PPLED_BACK_REG_B 16
H292	20.4V	PP_PWR	PWR	PPLED_OUT_A 35 37
H293	20.4V	PP_PWR	PWR	PPLED_OUT_B 35 37
H294	6.0V	PP_PWR	PWR	PPVBUS_PROT 36
H295	6.0V	PP_PWR	PWR	PPVBUS_USB 4 36
H296	6.0V	PP_PWR	PWR	PPVBUS_USB_DCIN 35 36
H297	5.0V	PP_PWR	PWR	PPVBUS_USB_PT_DK_CON 27 29
H298	1.8V	PP_PWR	PWR	PPVCCO_NAND 12
H299	4.7V	PP_PWR	PWR	PPVCC_MAIN 35 36 37
H300	0.6V	PP_PWR	PWR	PPVREF_DDR0_CA 13 44
H301	0.6V	PP_PWR	PWR	PPVREF_DDR0_DO 13 44
H302	0.6V	PP_PWR	PWR	PPVREF_DDR0_DO_H4 6
H303	0.6V	PP_PWR	PWR	PPVREF_DDR1_CA 13 44
H304	0.6V	PP_PWR	PWR	PPVREF_DDR1_DO 13 44
H305	0.6V	PP_PWR	PWR	PPVREF_DDR1_DO_H4 6
H306	0.6V	PP_PWR	PWR	PPVREF_DDR2_CA 14
H307	0.6V	PP_PWR	PWR	PPVREF_DDR2_DO 14
H308	0.6V	PP_PWR	PWR	PPVREF_DDR2_DO_H4 6
H309	0.6V	PP_PWR	PWR	PPVREF_DDR3_CA 14
H310	0.6V	PP_PWR	PWR	PPVREF_DDR3_DO 14
H311	0.6V	PP_PWR	PWR	PPVREF_DDR3_DO_H4 6
H312	4.6V	PP_PWR	PWR	BATT_POS_RC 36
H313	1.8V	PP_PWR	PWR	PP18V_GRAPE 17
H314	1.8V	PP_PWR	PWR	PP18V_R_GRAPE 17
H315		PP_PWR	PWR	DAC_AP_VREF 7
H316	3.3V	PP_PWR	PWR	PPVDDI_NAND_U1400 12
H317		PP_PWR	PWR	VR_BOOST_SW 17
H318		PP_PWR	PWR	VR_BOOST_L 17
H319	3.0V	PP_PWR	PWR	MT_3V3_INT 18 45

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND_PH	*	GND

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H290	GND	GND	VOLTAGE=0V	GND 19 21
H291	GND	GND	VOLTAGE=0V	GND_AUDIO_CODEC 19 21
H292	GND	GND	VOLTAGE=0V	GND_AUDIO_HP_AMP 21 27
H293	GND	GND	VOLTAGE=0V	GND_AUDIO_PT_DK 21 27
H294	GND	GND	VOLTAGE=0V	GND_SPKR_AMP1 20
H295	GND	GND	VOLTAGE=0V	GND_SPKR_AMP2 20
H296	GND	GND	VOLTAGE=0V	GND_PMU 17
H297	GND	GND		AGND 17
H298	GND	GND		AGND_U3000 17

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
H319		RST		BB_TRST_L 10
H320		RST		DBG_RST 10
H321		RST		DEBUG_RST_L 10
H322		RST		GSM_TXBURST_IND 5 15 30
H323		RST		JTAG_AP_TRST_L 4 10 42
H324		RST		RST_AP_IV8_L 4
H325		RST		RST_AP_L 4 27 30 37
H326		RST		RST_BB_L 5 30
H327		RST		RST_BB_PMU_L 10 37
H328		RST		RST_BT_L 15 37
H329		RST		RST_DET_L 5 30
H330		GRAPE		RST_GRAPE_L 4 17
H331		RST		RST_L63_L 19 37
H332		RST		RST_PMU_IN 4 37
H333		RST		RST_WLAN_L 15 37
H334		RST		SIMCRD_RST 10
H335		RST		TP_WLAN_TRST_L 10
H336		RST		UD881_RST 10
H337		RST		UD882_RST 10

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SNS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SNS	*	*	311_SPACING


NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_90D	*	90_OHM_DIFF

1E10	NC HSIC0_DATA2	NO_TEST=TRUE	4 42
1E11	NC HSIC0_STB2	NO_TEST=TRUE	4 42
1E12	NC HSIC1_DATA2	NO_TEST=TRUE	4 42
1E13	NC HSIC1_STB2	NO_TEST=TRUE	4 42
1E14	NC JTAG_AP_TRICK	NO_TEST=TRUE	4
1E15	NC USB_D1_P	NO_TEST=TRUE	4 42
1E16	NC USB_D1_N	NO_TEST=TRUE	4 42
1E17	NC USB11_D1_P	NO_TEST=TRUE	4 42
1E18	NC USB11_D1_N	NO_TEST=TRUE	4 42
1E19	NC USB_ANALOGTEST0	NO_TEST=TRUE	4
1E20	NC USB_ANALOGTEST1	NO_TEST=TRUE	4
1E21	NC USB_ID0	NO_TEST=TRUE	4
1E22	NC USB_ID1	NO_TEST=TRUE	4
1E23	NC USB_BRICKID1	NO_TEST=TRUE	4
1E24	NC I2S1_MCK	NO_TEST=TRUE	5
1E25	NC I2S1_BCLK	NO_TEST=TRUE	5
1E26	NC I2S1_LBCK	NO_TEST=TRUE	5
1E27	NC I2S1_DIN	NO_TEST=TRUE	5
1E28	NC I2S1_DOUT	NO_TEST=TRUE	5
1E29	NC I2S2_MCK	NO_TEST=TRUE	5
1E30	NC I2S3_MCK	NO_TEST=TRUE	5
1E31	NC AP_GPIO216	NO_TEST=TRUE	5
1E32	NC SPI_FLASH_CS_L	NO_TEST=TRUE	5
1E33	NC SWI_AP	NO_TEST=TRUE	5
1E34	NC SDIO0_WL_CLK	NO_TEST=TRUE	5
1E35	NC SDIO0_WL_CMD	NO_TEST=TRUE	5
1E36	NC SDIO0_WL_DATA<0>	NO_TEST=TRUE	5
1E37	NC SDIO0_WL_DATA<1>	NO_TEST=TRUE	5
1E38	NC SDIO0_WL_DATA<2>	NO_TEST=TRUE	5
1E39	NC SDIO0_WL_DATA<3>	NO_TEST=TRUE	5
1E40	NC SPI3_MISO	NO_TEST=TRUE	5
1E41	NC SPI3_MOSI	NO_TEST=TRUE	5
1E42	NC SPI3_SCLK	NO_TEST=TRUE	5
1E43	NC SPI3_CS_L	NO_TEST=TRUE	5
1E44	NC AP_GPIO3	NO_TEST=TRUE	5
1E45	NC AP_GPIO7	NO_TEST=TRUE	5
1E46	NC AP_GPIO8	NO_TEST=TRUE	5
1E47	NC AP_GPIO11	NO_TEST=TRUE	5
1E48	NC AP_GPIO13	NO_TEST=TRUE	5
1E49	NC BOARD_ID_3	NO_TEST=TRUE	5
1E50	NC AP_GPIO19	NO_TEST=TRUE	5
1E51	NC AP_GPIO31	NO_TEST=TRUE	5
1E52	NC AP_GPIO35	NO_TEST=TRUE	5
1E53	NC AP_GPIO3V1	NO_TEST=TRUE	5
1E54	NC AP_GPIO185	NO_TEST=TRUE	5
1E55	NC AP_GPIO186	NO_TEST=TRUE	5
1E56	NC UART2_RXD	NO_TEST=TRUE	5
1E57	NC UART2_TXD	NO_TEST=TRUE	5
1E58	NC UART4_CTS_L	NO_TEST=TRUE	5
1E59	NC UART4_RTS_L	NO_TEST=TRUE	5
1E60	NC UART4_RXD	NO_TEST=TRUE	5
1E61	NC UART4_TXD	NO_TEST=TRUE	5
1E62	NC UART6_CTSN	NO_TEST=TRUE	5
1E63	NC UART6_RTSN	NO_TEST=TRUE	5

1E14	NC FMI0_CE2_L	NO_TEST=TRUE	6
1E15	NC FMI0_CE3_L	NO_TEST=TRUE	6
1E16	NC FMI0_CE4_L	NO_TEST=TRUE	6
1E17	NC FMI0_CE5_L	NO_TEST=TRUE	6
1E18	NC FMI0_CE6_L	NO_TEST=TRUE	6
1E19	NC FMI0_CE7_L	NO_TEST=TRUE	6
1E20	NC FMI1_CE2_L	NO_TEST=TRUE	6
1E21	NC FMI1_CE3_L	NO_TEST=TRUE	6
1E22	NC FMI1_CE4_L	NO_TEST=TRUE	6
1E23	NC FMI1_CE5_L	NO_TEST=TRUE	6
1E24	NC FMI1_CE6_L	NO_TEST=TRUE	6
1E25	NC FMI1_CE7_L	NO_TEST=TRUE	6
1E26	NC FMI2_CE1_L	NO_TEST=TRUE	6
1E27	NC FMI2_CE2_L	NO_TEST=TRUE	6
1E28	NC FMI2_CE3_L	NO_TEST=TRUE	6
1E29	NC FMI2_CE5_L	NO_TEST=TRUE	6
1E30	NC FMI2_AD<0>	NO_TEST=TRUE	6
1E31	NC FMI2_AD<1>	NO_TEST=TRUE	6
1E32	NC FMI2_AD<2>	NO_TEST=TRUE	6
1E33	NC FMI2_AD<3>	NO_TEST=TRUE	6
1E34	NC FMI2_AD<4>	NO_TEST=TRUE	6
1E35	NC FMI2_AD<5>	NO_TEST=TRUE	6
1E36	NC FMI2_AD<6>	NO_TEST=TRUE	6
1E37	NC FMI2_AD<7>	NO_TEST=TRUE	6
1E38	NC FMI2_ALE	NO_TEST=TRUE	6
1E39	NC FMI2_CLE	NO_TEST=TRUE	6
1E40	NC FMI2_WE_L	NO_TEST=TRUE	6
1E41	NC FMI2_RE_L	NO_TEST=TRUE	6
1E42	NC FMI2_DQS	NO_TEST=TRUE	6
1E43	NC FMI3_CE0_L	NO_TEST=TRUE	6
1E44	NC FMI3_CE1_L	NO_TEST=TRUE	6
1E45	NC FMI3_CE2_L	NO_TEST=TRUE	6
1E46	NC FMI3_CE3_L	NO_TEST=TRUE	6
1E47	NC FMI3_CE4_L	NO_TEST=TRUE	6
1E48	NC FMI3_CE5_L	NO_TEST=TRUE	6
1E49	NC FMI3_CE6_L	NO_TEST=TRUE	6
1E50	NC FMI3_CE7_L	NO_TEST=TRUE	6
1E51	NC FMI3_AD<0>	NO_TEST=TRUE	6
1E52	NC FMI3_AD<1>	NO_TEST=TRUE	6
1E53	NC FMI3_AD<2>	NO_TEST=TRUE	6
1E54	NC FMI3_AD<3>	NO_TEST=TRUE	6
1E55	NC FMI3_AD<4>	NO_TEST=TRUE	6
1E56	NC FMI3_AD<5>	NO_TEST=TRUE	6
1E57	NC FMI3_AD<6>	NO_TEST=TRUE	6
1E58	NC FMI3_AD<7>	NO_TEST=TRUE	6
1E59	NC FMI3_ALE	NO_TEST=TRUE	6
1E60	NC FMI3_CLE	NO_TEST=TRUE	6
1E61	NC FMI3_WE_L	NO_TEST=TRUE	6
1E62	NC FMI3_RE_L	NO_TEST=TRUE	6
1E63	NC FMI3_DQS	NO_TEST=TRUE	6
1E64	NC MIPI_VSYNC_H4	NO_TEST=TRUE	7
1E65	NC MIPI0C_AP_DATA_P<2>	NO_TEST=TRUE	7 43
1E66	NC MIPI0C_AP_DATA_N<2>	NO_TEST=TRUE	7 43
1E67	NC MIPI0C_AP_DATA_P<3>	NO_TEST=TRUE	7 43
1E68	NC MIPI0C_AP_DATA_N<3>	NO_TEST=TRUE	7 43
1E69	NC MIPI1C_AP_DATA_P<1>	NO_TEST=TRUE	7 43
1E70	NC MIPI1C_AP_DATA_N<1>	NO_TEST=TRUE	7 43
1E71	NC ISP_AP_1_FLASH	NO_TEST=TRUE	7
1E72	NC ISP_AP_1_PRE_FLASH	NO_TEST=TRUE	7

1E10	NC DDR0_CKE<1>	NO_TEST=TRUE	8
1E11	NC DDR1_CKE<1>	NO_TEST=TRUE	8
1E12	NC DDR2_CKE<1>	NO_TEST=TRUE	8
1E13	NC DDR3_CKE<1>	NO_TEST=TRUE	8
1E14	NC DDR0_CSN<1>	NO_TEST=TRUE	8
1E15	NC DDR1_CSN<1>	NO_TEST=TRUE	8
1E16	NC DDR2_CSN<1>	NO_TEST=TRUE	8
1E17	NC DDR3_CSN<1>	NO_TEST=TRUE	8
1E18	NC PMU_VBUCK0_SW0_G	NO_TEST=TRUE	36
1E19	NC PMU_VBUCK0_SW0_S	NO_TEST=TRUE	36
1E20	NC VBUS_A_OV_L	NO_TEST=TRUE	36
1E21	NC BOARD_TEMP7	NO_TEST=TRUE	37
1E22	NC BOARD_TEMP8	NO_TEST=TRUE	37
1E23	NC PMU_GPIO12	NO_TEST=TRUE	37
1E24	NC PMU_GPIO13	NO_TEST=TRUE	37
1E25	NC PMU_GPIO16	NO_TEST=TRUE	37
1E26	NC PMU_GPIO17	NO_TEST=TRUE	37
1E27	NC PMU_AMUX_A0	NO_TEST=TRUE	37
1E28	NC PMU_AMUX_A1	NO_TEST=TRUE	37
1E29	NC PMU_AMUX_A2	NO_TEST=TRUE	37
1E30	NC PMU_AMUX_A3	NO_TEST=TRUE	37
1E31	NC PMU_AMUX_AY	NO_TEST=TRUE	37
1E32	NC PMU_AMUX_B0	NO_TEST=TRUE	37
1E33	NC PMU_AMUX_B1	NO_TEST=TRUE	37
1E34	NC PMU_AMUX_B2	NO_TEST=TRUE	37
1E35	NC PMU_AMUX_B3	NO_TEST=TRUE	37
1E36	NC PMU_AMUX_BY	NO_TEST=TRUE	37

1E20	NC BON_L1	NO_TEST=TRUE	18
1E21	NC BON_L3	NO_TEST=TRUE	18
1E22	NC BON_L5	NO_TEST=TRUE	18
1E23	NC EAROUT_AP	NO_TEST=TRUE	19
1E24	NC EAROUT_AN	NO_TEST=TRUE	19
1E25	NC LINE_IN1_CODEC	NO_TEST=TRUE	19
1E26	NC LINE_IN1_REF_CODEC	NO_TEST=TRUE	19
1E27	NC LINE_IN2_CODEC	NO_TEST=TRUE	19
1E28	NC LINE_IN2_REF_CODEC	NO_TEST=TRUE	19
1E29	NC MIC1_BIAS_CODEC	NO_TEST=TRUE	19
1E30	NC MIC1P_CODEC	NO_TEST=TRUE	19
1E31	NC MIC1N_CODEC	NO_TEST=TRUE	19
1E32	NC MIC1_FILT_CODEC	NO_TEST=TRUE	19
1E33	NC D5703_6	NO_TEST=TRUE	37
1E34	NC D5700_6	NO_TEST=TRUE	37
1E35	NC D5701_6	NO_TEST=TRUE	37
1E36	NC D5702_6	NO_TEST=TRUE	37
1E37	NC LCM2_EN	NO_TEST=TRUE	37
1E38	NC VLCM1	NO_TEST=TRUE	37

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