

ZZZ



PCB DAZ@  
DA8000WY000  
PCB 10G LA-A401P REV0 M/B HDI 1

S1



FRAME  
ECOMV000200

@

S4



FRAME  
ECOMV000200  
for GLONASS

@

# Compal Confidential

## Schematics Document

### ZSJVV

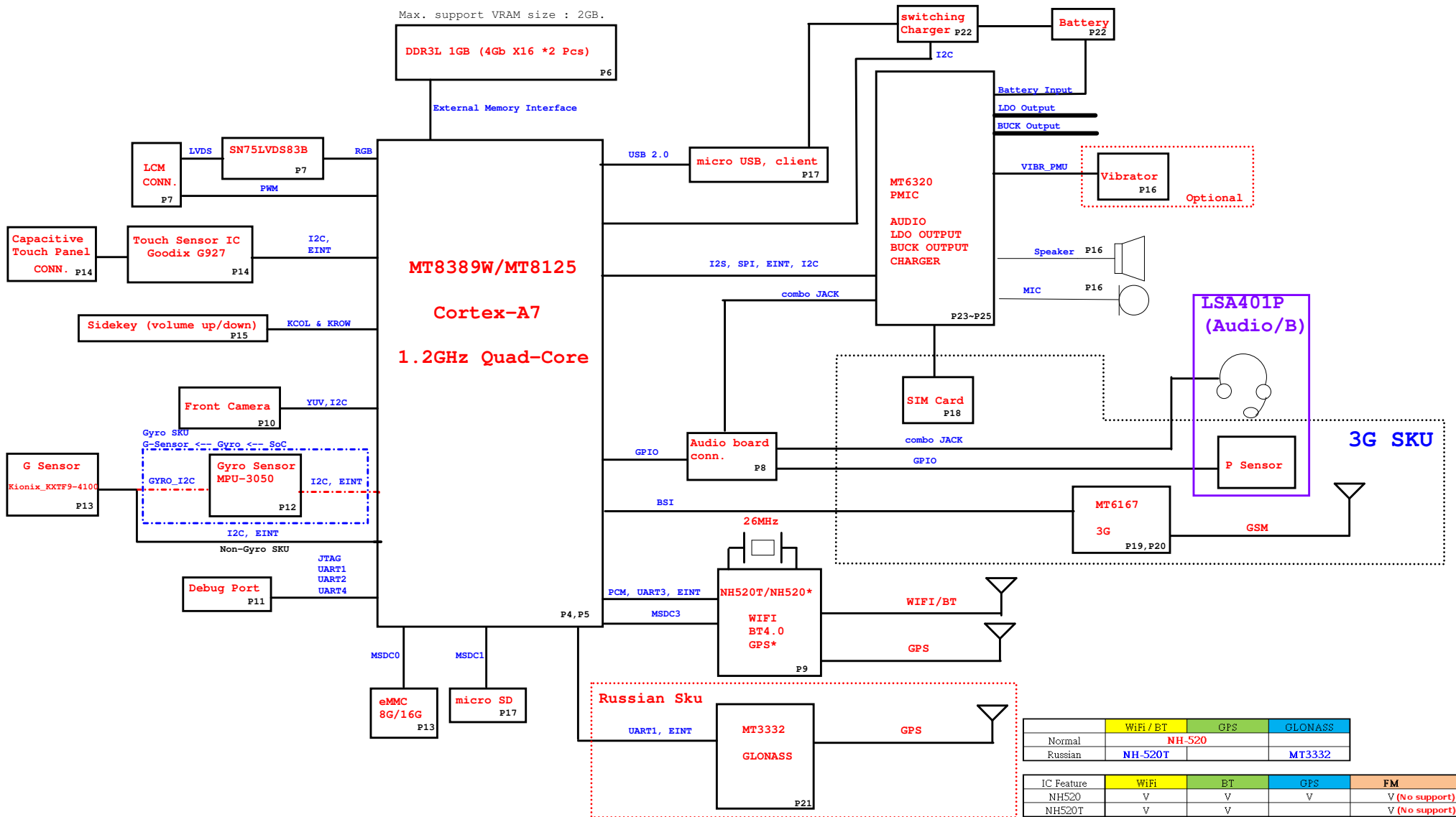
### LA-A401P

2013-02-26

REV:0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/11/09	Deciphered Date	2014/11/09	Title	Cover Page
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# giordano2 block diagram



	WIFI / BT	GPS	GLONASS
Normal		NH-520	
Russian	NH-520T		MT3332

IC Feature	WIFI	BT	GPS	FM
NH520	v		v	v (No support)
NH520T	v	v		v (No support)

## Voltage Rails

MT6320 Power Plane	Function	Power Level	IDLE	Sleep mode
VCORE_PMU	VCORE switching output	0.75 ~ 1.3	ON	Low voltage
VPROC_PMU	VPROC switching output	0.75 ~ 1.3	ON	Low voltage
VTCXO_1_PMU	LDO output for TCXO	2.8V	ON	OFF
VCAMA_PMU	LDO output for camera analog	2.8V	ON	Gating by SW
VSRAM_PMU	LDO output used for 1.2V SRAM	1.2V	ON	Low voltage
VDD28_6583	LDO output used for 2.8V IO	2.8V	ON	Gating by SW
VGP2_PMU	LDO output for camera 1.8V	1.8V	ON	Gating by SW
VEMC_3V3_PMU	LDO output for eMMC&P-sensor	3.3V	ON	Gating by SW
VMCH_PMU	LDO output for SD card	3.3V	ON	Gating by SW
VGP5_PMU	LDO output for Touch panel	2.8V	ON	Gating by SW
DDR3VCCIO	LDO output for DDR3L	1.35V	ON	Gating by SW
VDD33_6583	LCD & Bridge power	3.3V	ON	Gating by SW
VDD18_6583	LDO output used for 1.8V IO	1.8V	ON	Gating by SW
VRF18_PMU	LDO output for RF_MT6167	1.8V	ON	Gating by SW

## Main board ID

MB_ID0	MB_ID1	
0	0	EVT
0	1	DVT
1	0	PVT
1	1	MP

## I2C address

Device	Address(7 bit)	Address(8bit)	
		Write	Read
Gyro (MPU-3050)	0x68	0xD0	0xD1
G-sensor (KXTIK-1004)	0x0F	0x1E	0x1F
Touch screen (GT927)	0x5D	0xBA	0xBB
Camera (OV7675)	0x21	0x42	0x43
Charge (BQ24196 )	0x6B	0xD6	0xD7
G-sensor(KXTIK-1004)	0x0F	0x1E	0x1F
PMU(MT6320)			

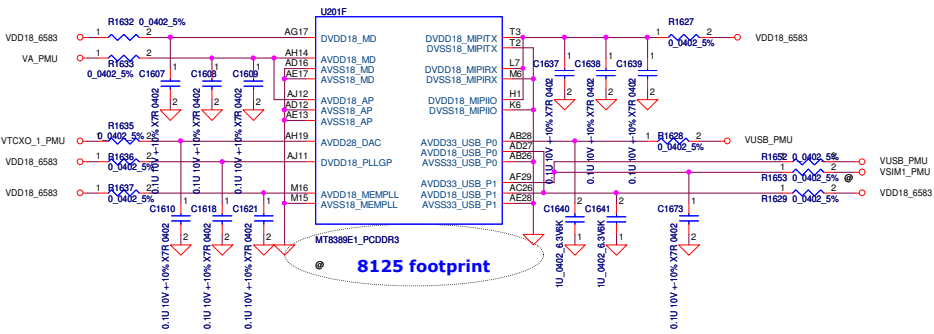
## BOM structure

Name	Function	
3G@	3G only	
WIFI_ONLY@	WIFI ONLY	
DAZ@	PCB	
EMC@	for EMC request	
NH520@	AW-NH520	
NH520_EM@	GPS EMC	
GLONASS@	MT3332	

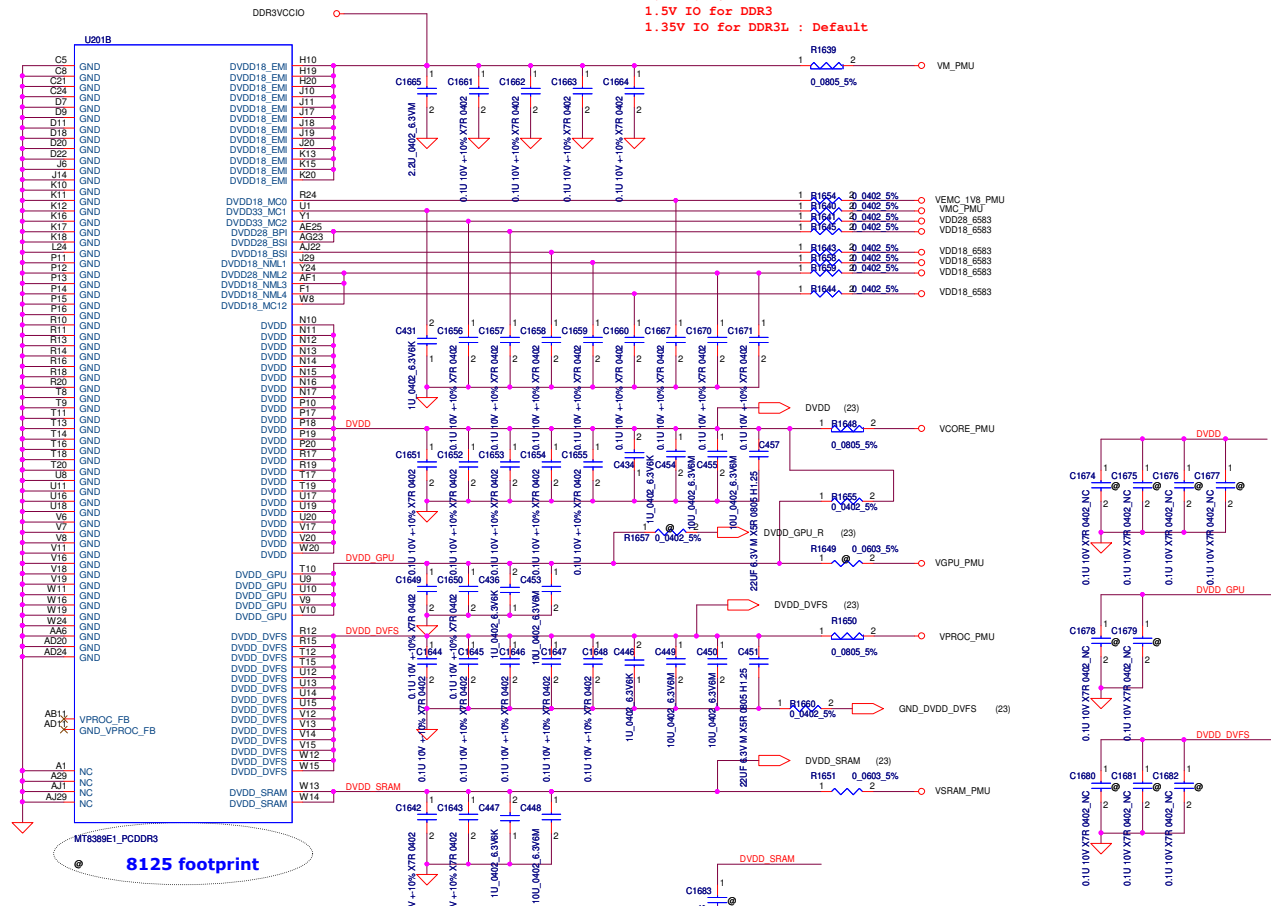
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U201  
36@  
**SA00006SG00**  
S IC MT8389WK/A 1.2G FCCSP 515P CPU

U201  
WIFI\_ONLY@  
**SA00006S500**  
S IC MT8389WK/A 1.2G FCCSP 515P CPU

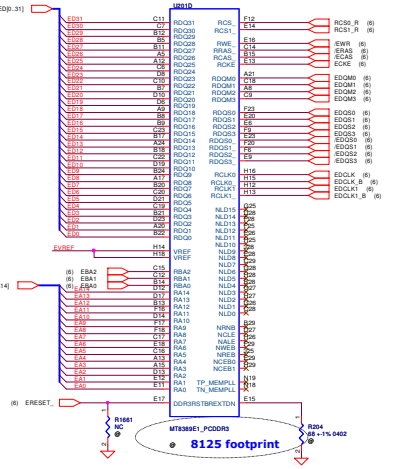
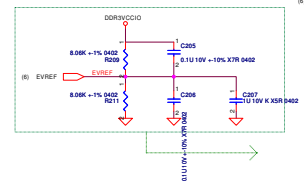
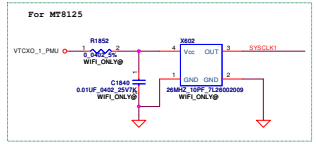
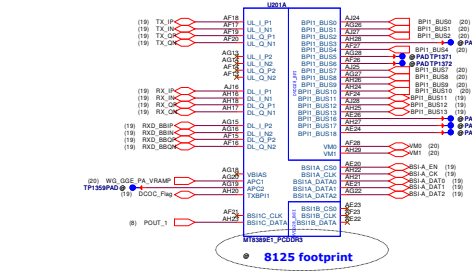
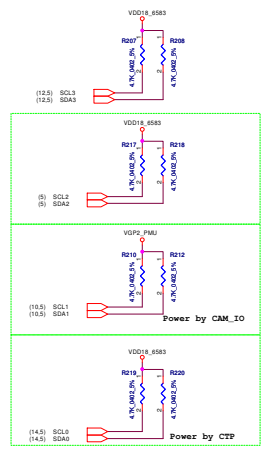
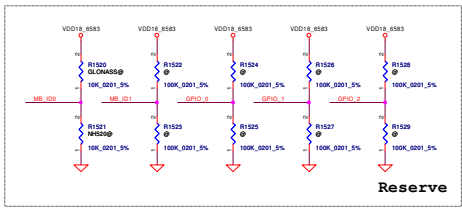


1.8V IO for DDR  
1.2V IO for DDR2  
1.5V IO for DDR3  
1.35V IO for DDR3L : Default

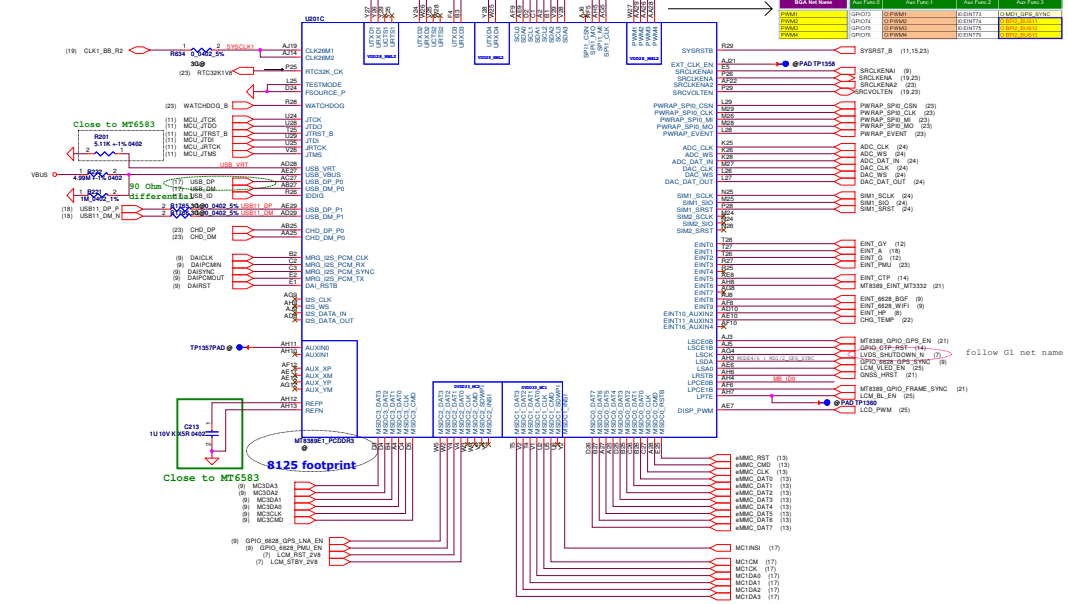


MT8389E1\_PCCDDR3  
8125 footprint

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<TESTMODE>  
Connect to VDDIO : Enter Test Mode  
Connect to GND : Normal mode  
  
<#SOURCE\_P>  
Connect to VDDP (2V0) : w/1 SPSSE program  
Connect to GND : w/0 SPSSE program



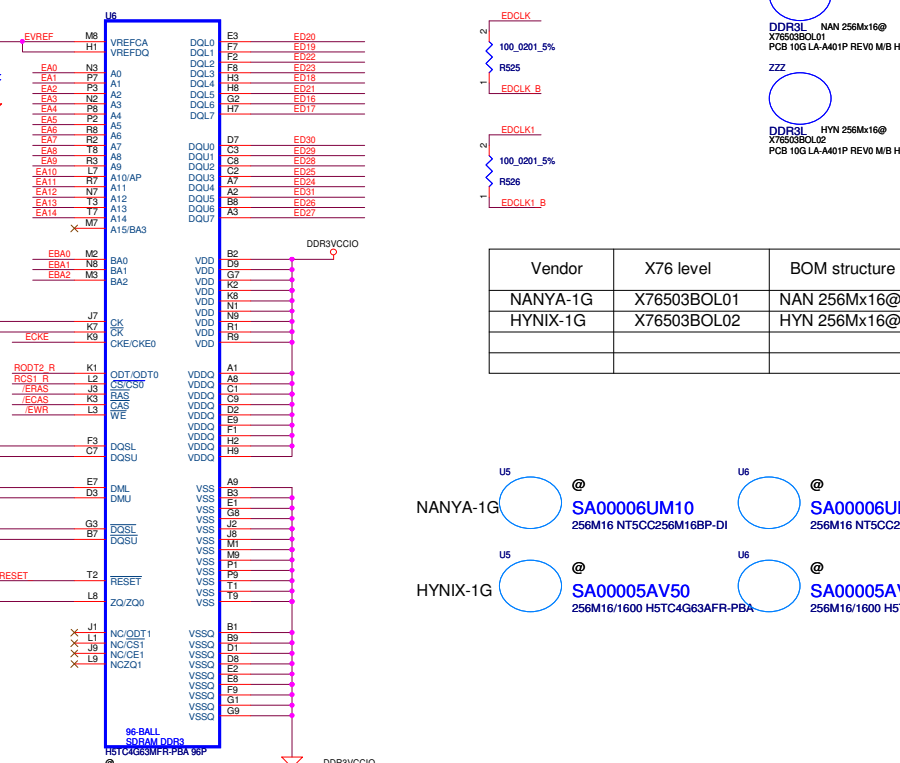
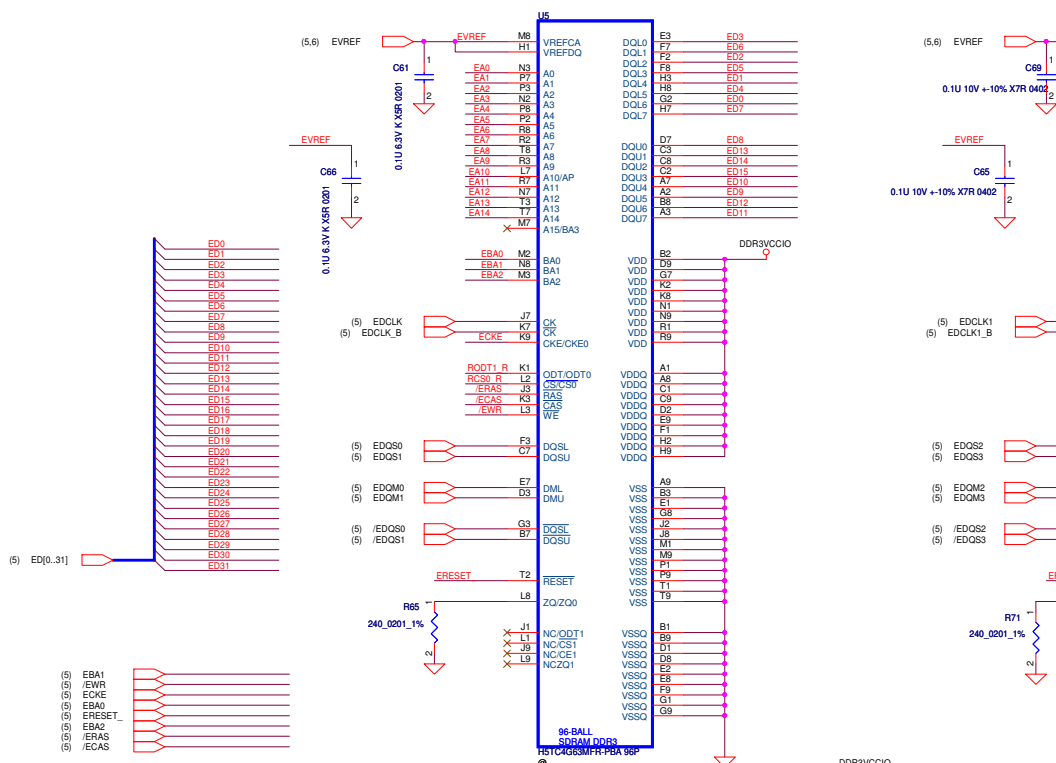
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 8125: I2C  
 8125: -Sensor  
 8125: SPM0 HW3300  
 8125: CTP  
 8125: MT6628  
 8125: MT6628 WIFL  
 8125: HEADSET

1200 : CTP  
 1201 : Sub Camera  
 1202 : G/GYRO sensor  
 1204 (PMIC) : Charger IC  
 1205 (PMIC) :  
 1206 (PMIC) :

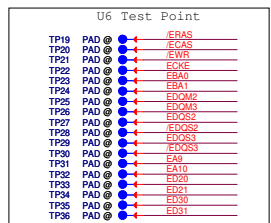
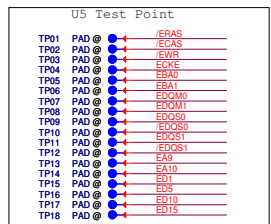
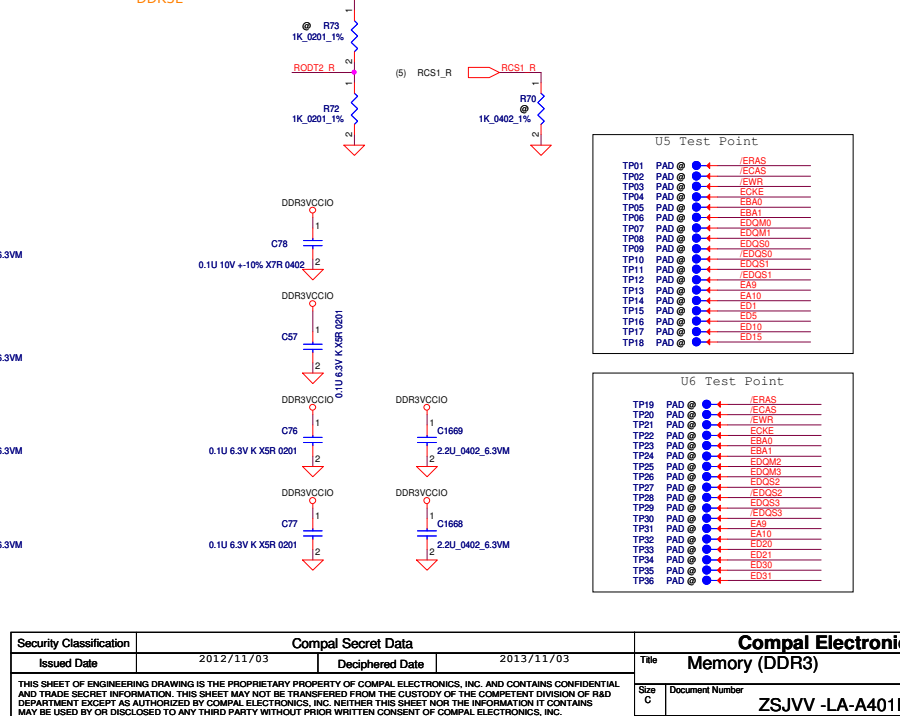
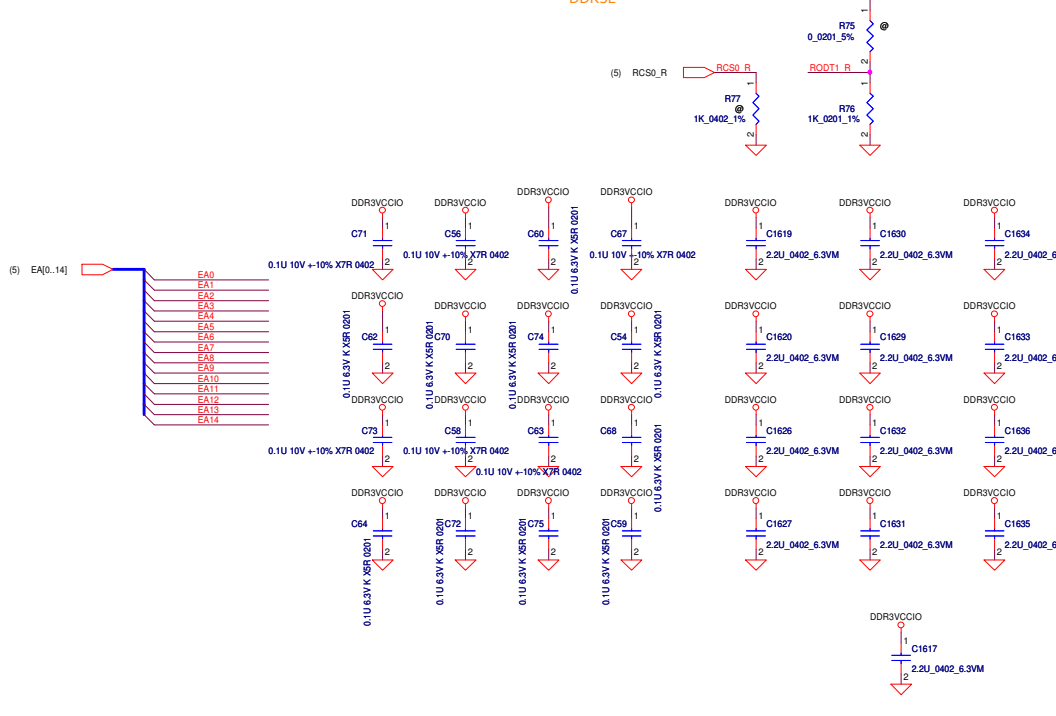
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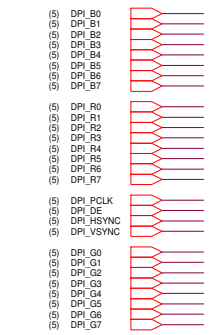
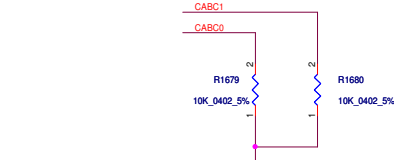
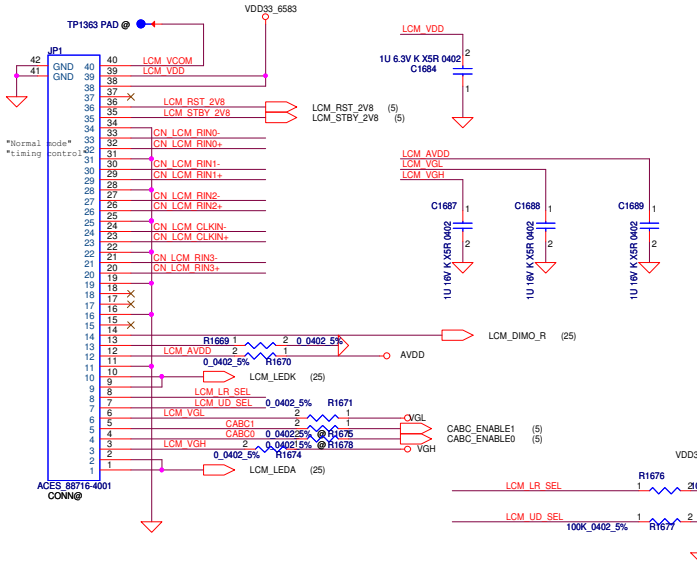
MDSD0 : eMMC  
 MDSD1 : SD Card  
 MDSD2 : GPIO (2.8V)  
 MDSD3 : MT6628

Security Classification	Compel Secret Data		Compel Electronics, Inc.
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Item	MT8377 - Baseband		Rev
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Doc ID	ZSJVV-LA-A401P		Rev
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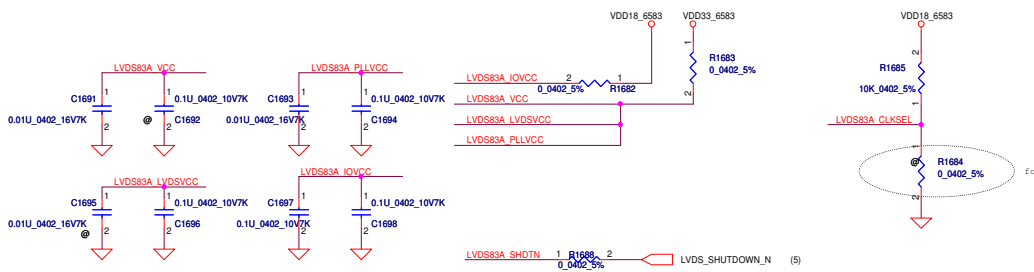
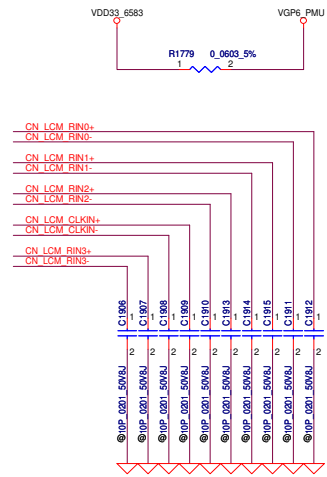
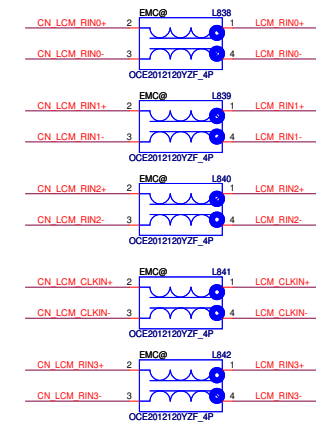
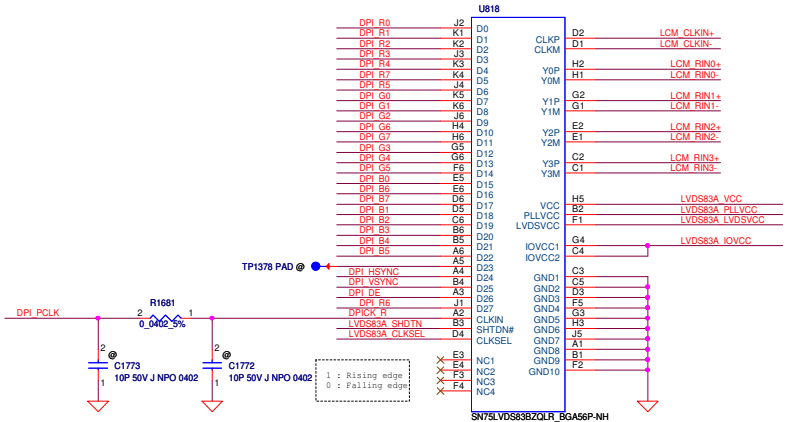


Vendor	X76 level	BOM structure
NANYA-1G	X76503BOL01	NAN 256Mx16@
HYNIX-1G	X76503BOL02	HYN 256Mx16@



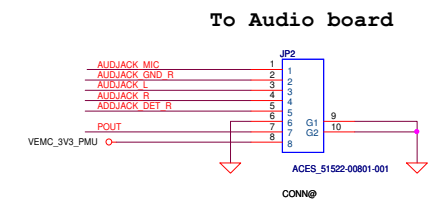
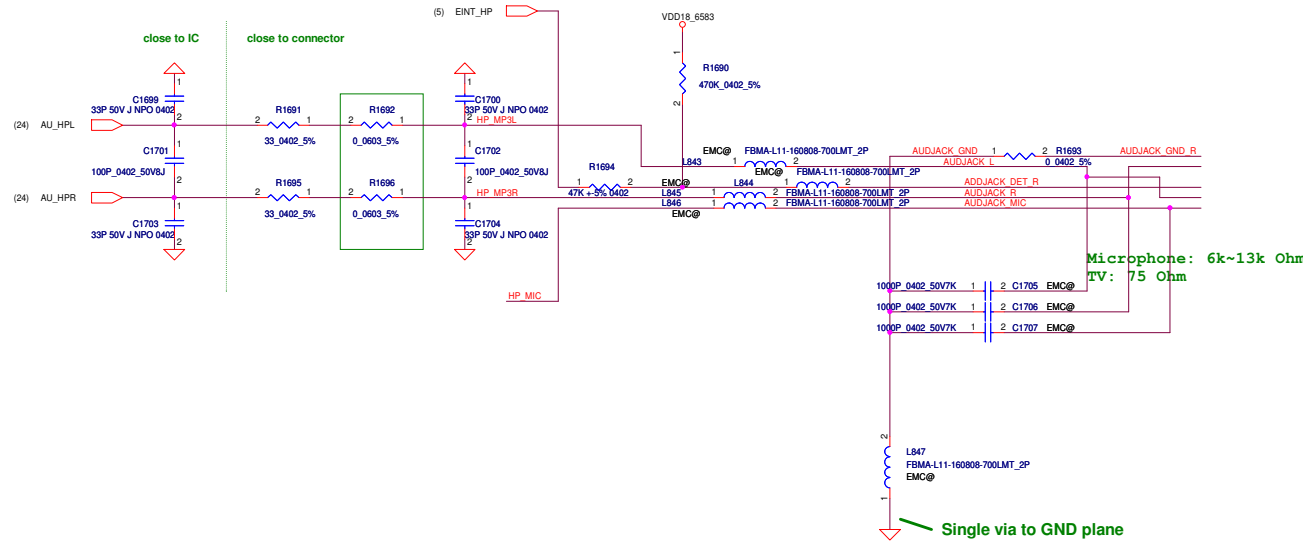


### LVDS Bridge

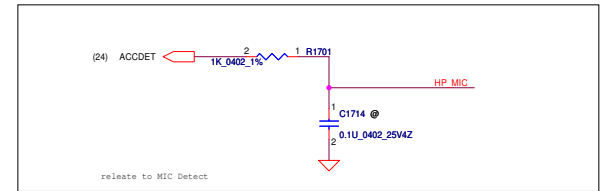
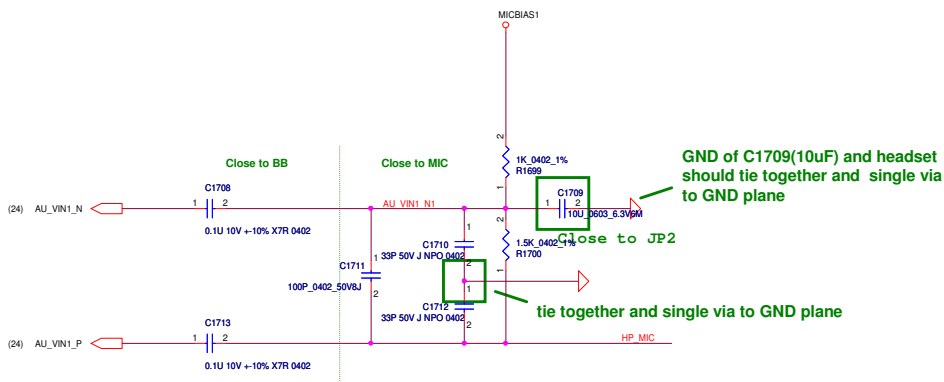


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# Earphone RECEIVER

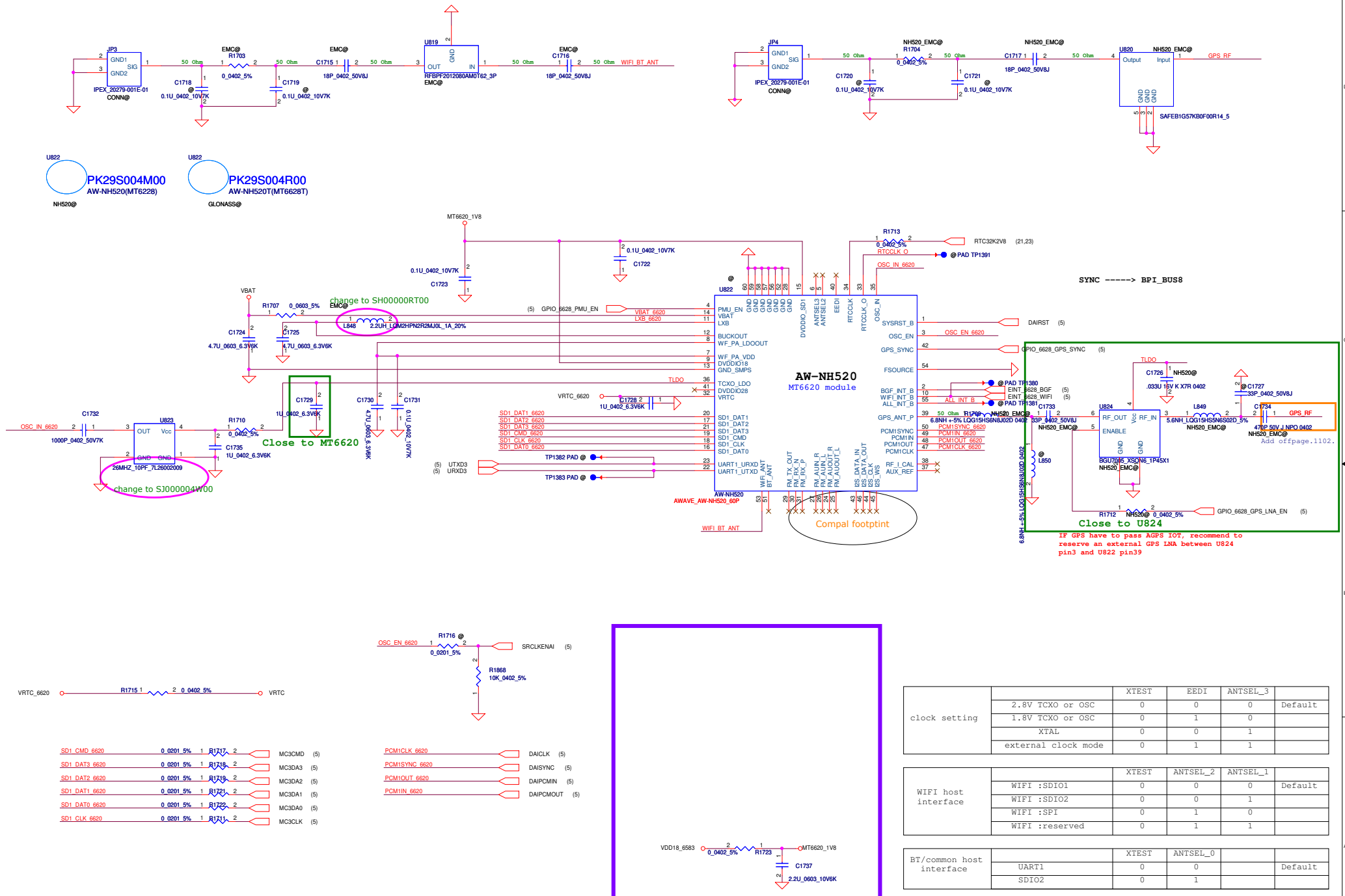


# Earphone MICPHONE



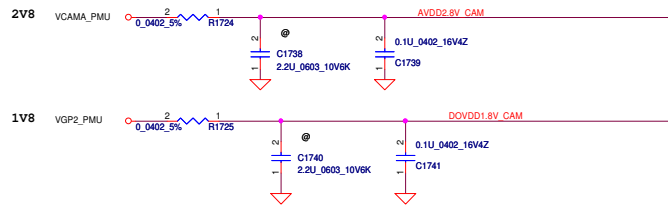
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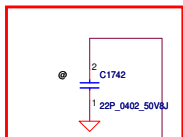


	XTEST	EEDI	ANTSEL_3	
clock setting	2.8V TCXO or OSC	0	0	Default
	1.8V TCXO or OSC	0	1	0
	XTAL	0	0	1
	external clock mode	0	1	1
WIFI host interface	WIFI :SDIO1	0	0	Default
	WIFI :SDIO2	0	0	1
	WIFI :SPI	0	1	0
	WIFI :reserved	0	1	1
BT/common host interface	UART1	0	0	Default
	SDIO2	0	1	

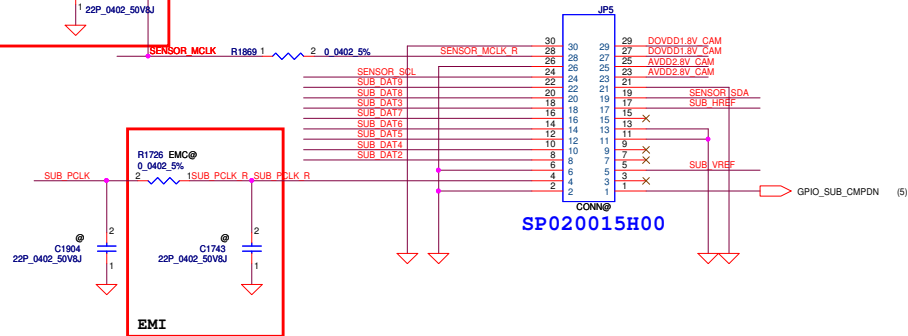
# Sub Camera



Acer reserve

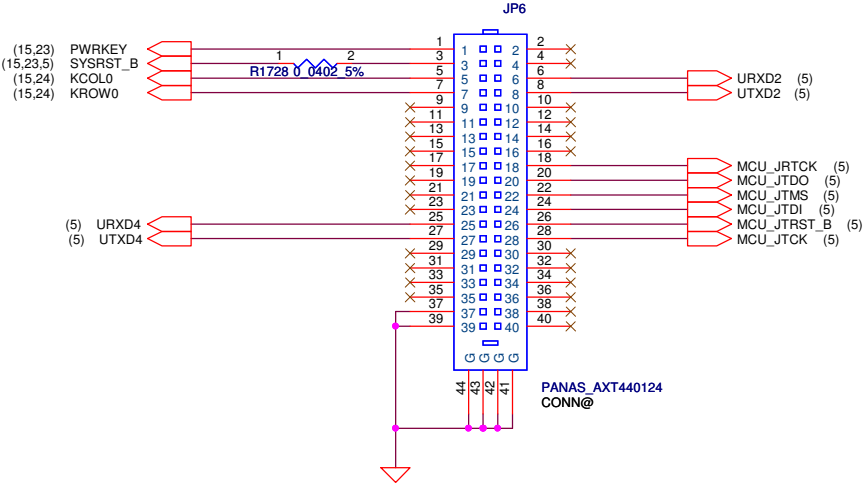


0.3M connector



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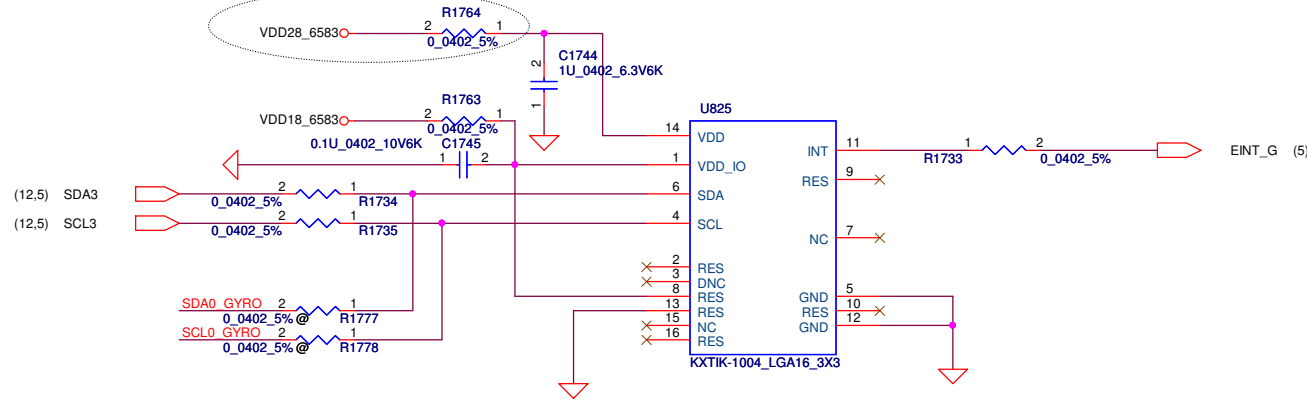
# Common Debug



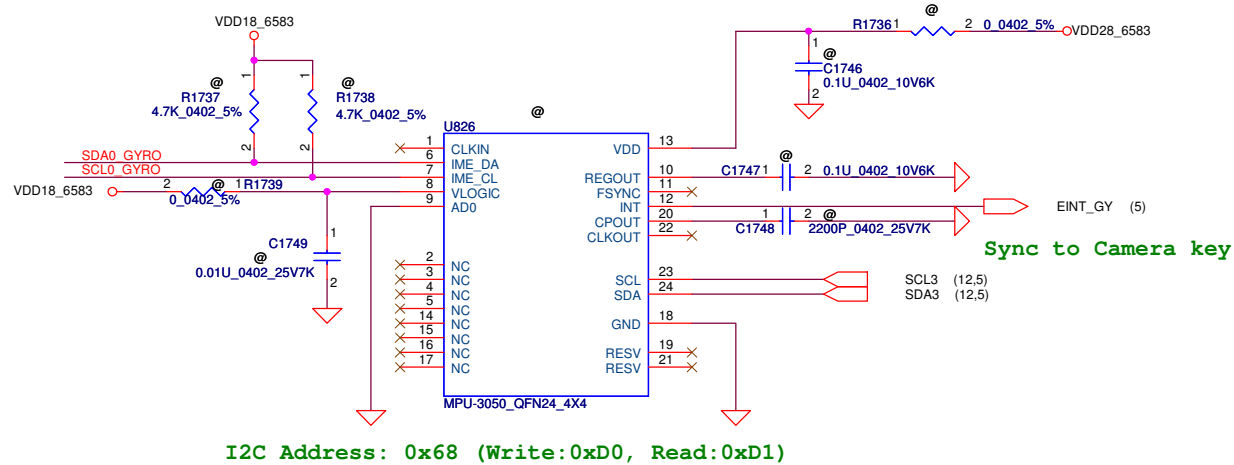
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# G-Sensor

for co-lay STK8313

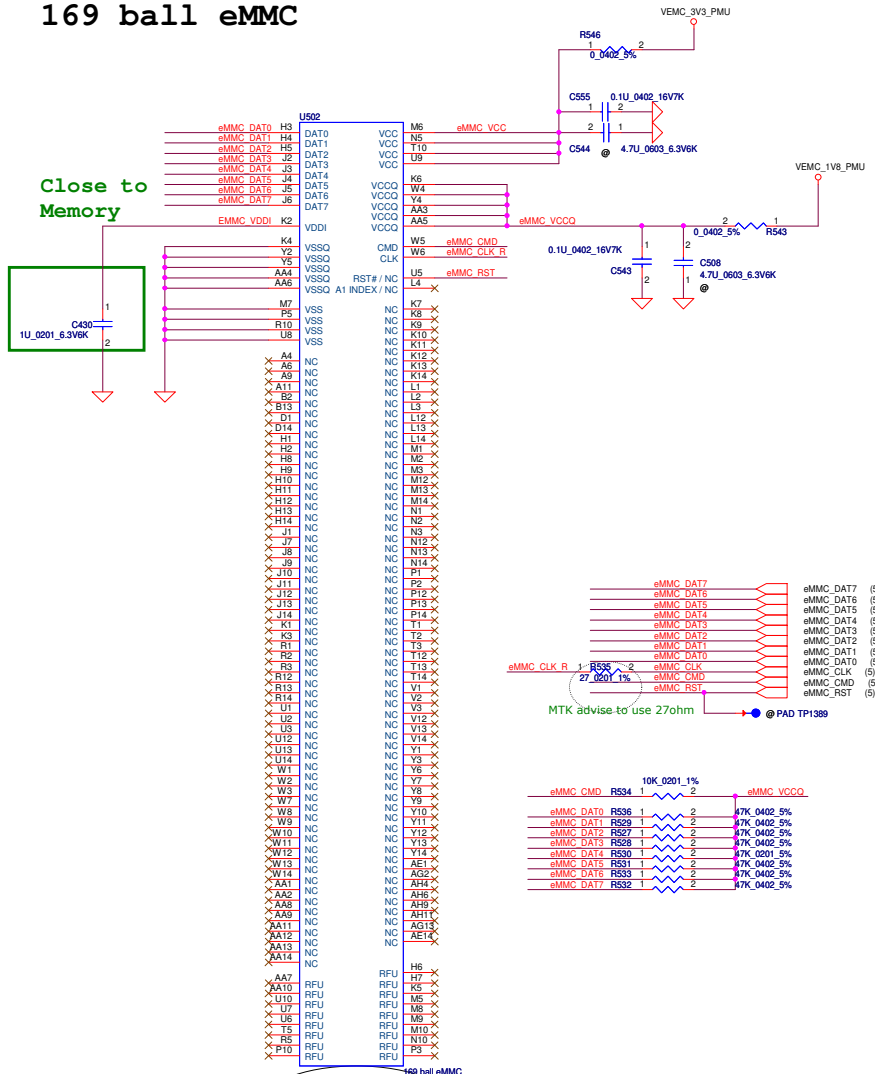


# Gyro Sensor

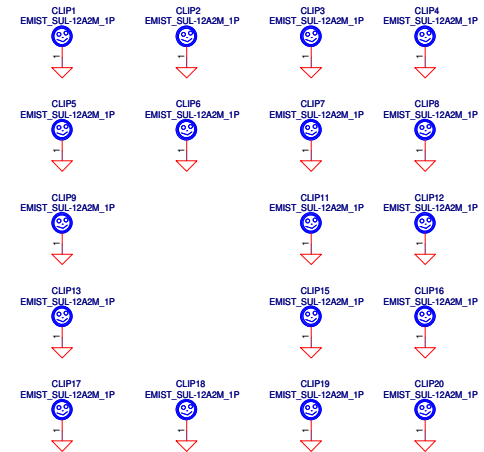
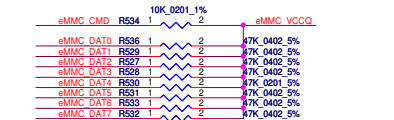
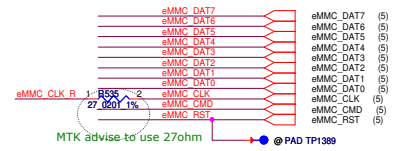


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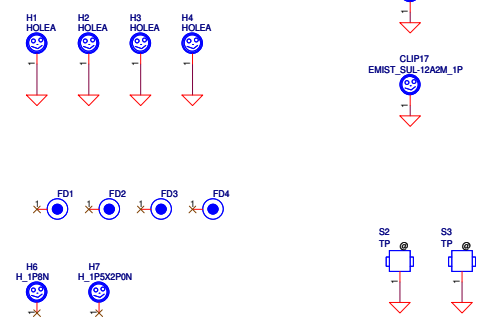
# 169 ball eMMC



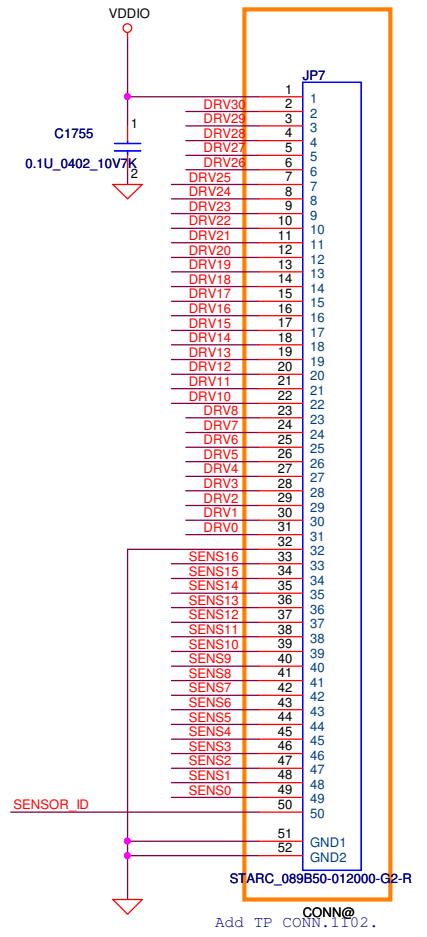
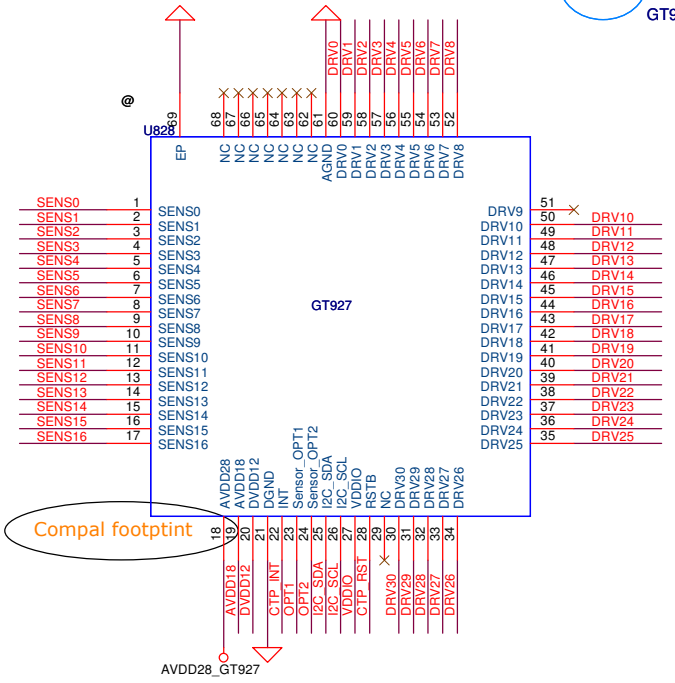
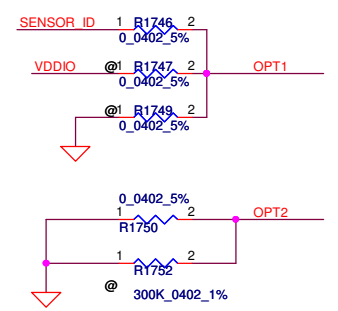
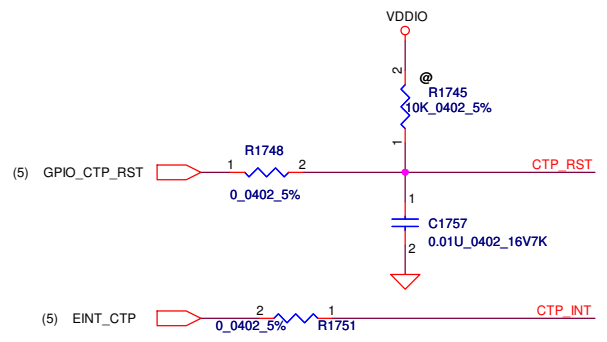
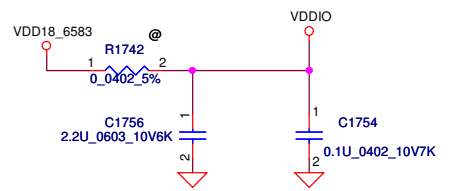
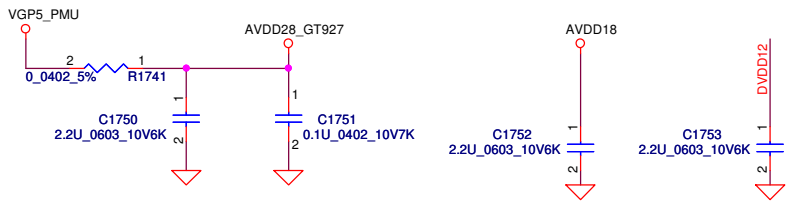
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| <p>U502 KIN 8GB@<br/>SA00006MF30<br/>Kingston 8G KE4CN3K6A</p>   | <p>U502 KIN 16GB@<br/>SA00006MG30<br/>Kingston 16G KE4CN4K6A</p>  |
| <p>U502 HYN 8GB@<br/>SA00006PW10<br/>HYNIX 8G H26M42002GMR</p>   | <p>U502 HYN 16GB@<br/>SA00006VJ10<br/>HYNIX 16G H26M52002EQR</p>  |
| <p>U502 SAM 8GB@<br/>SA00006VE10<br/>Samsung KLM8G1WE4A-A001</p> | <p>U502 SAM 16GB@<br/>SA00006Z610<br/>Samsung KLMAG2WE4A-A001</p> |



## SCREW HOLE

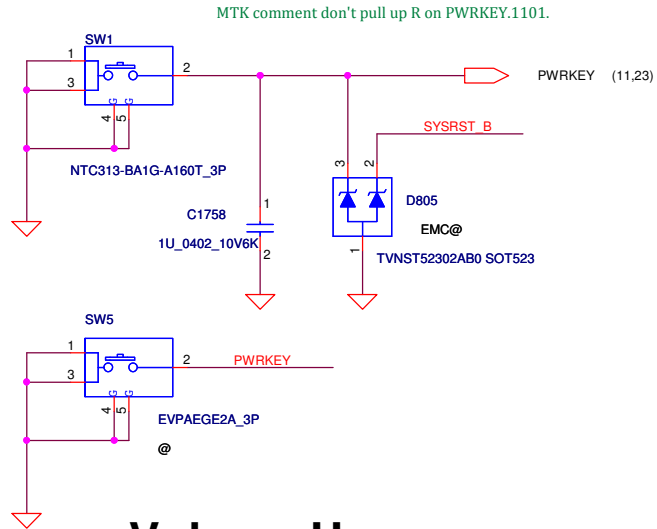


SDIN4E2-16G-T\_TFBGA\_169P  
© ompal footptint



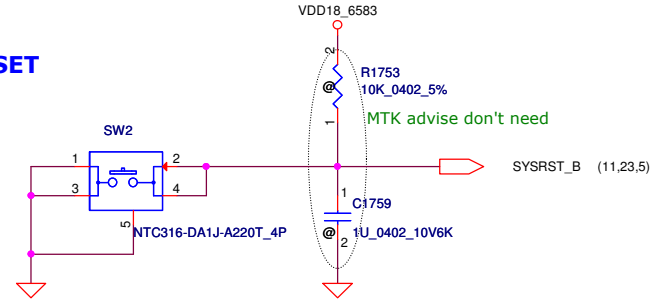
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### Power-on Button

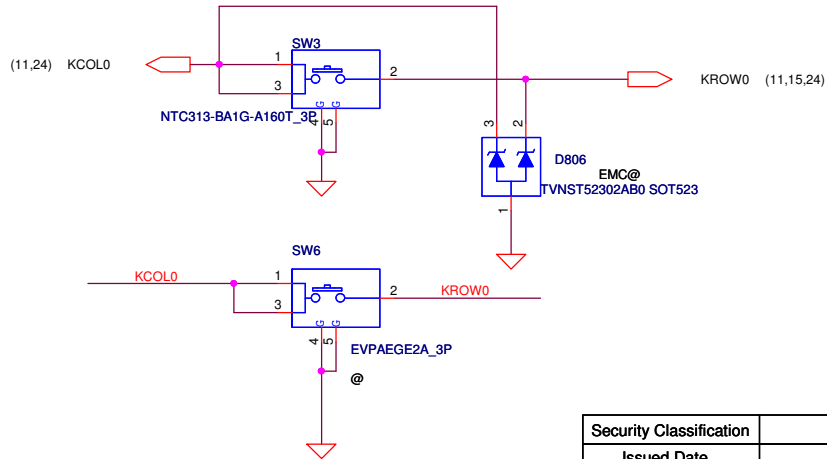


### Compal GND MTK GND

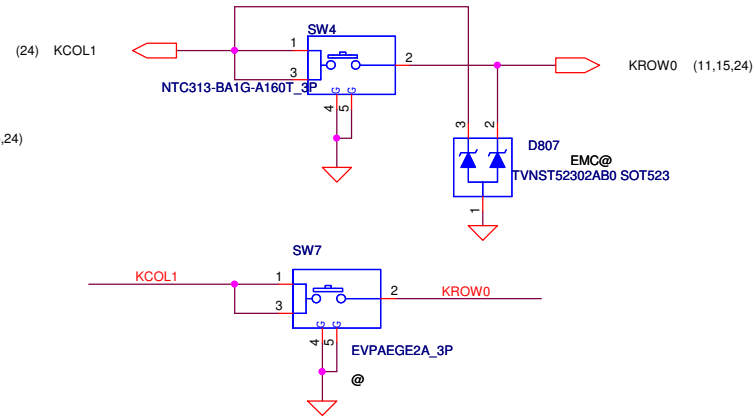
### RESET



### Volume Up (Download Key)

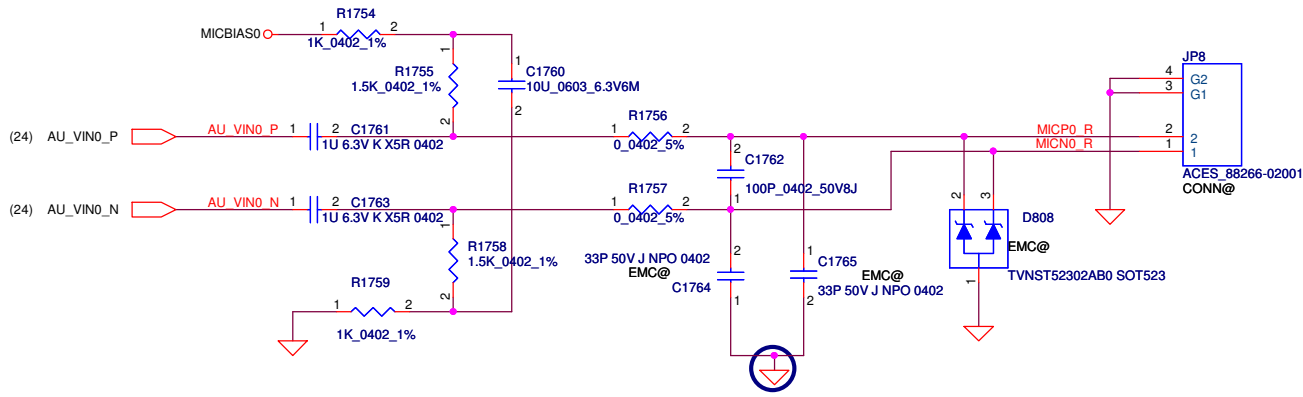


### Volume Down

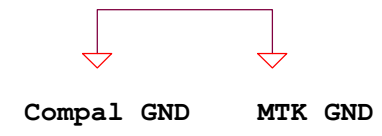


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Issued Date	2012/11/03	Deciphered Date	2013/11/03	Title Button
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				Rev 0.1

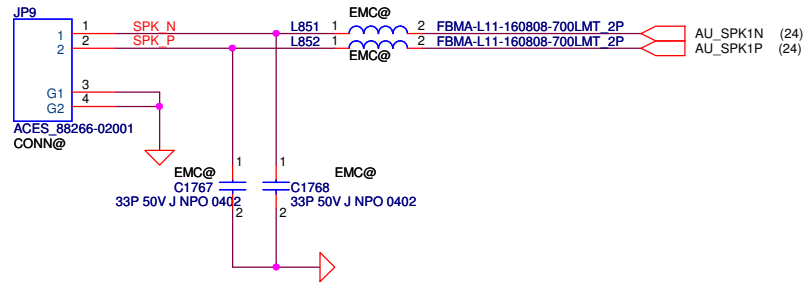
# MIC



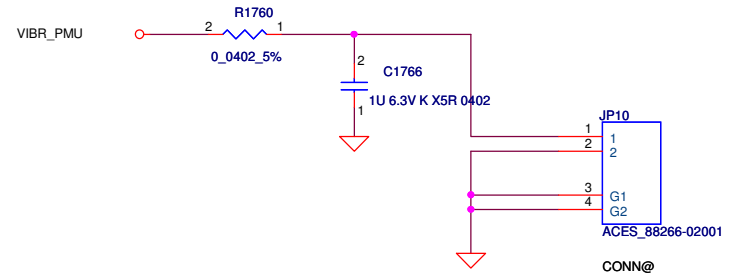
Modify MIC CONN SCH.1102.



# SPAKER



# Vibrator



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				ZSJVV-LA-A401P
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				0.1
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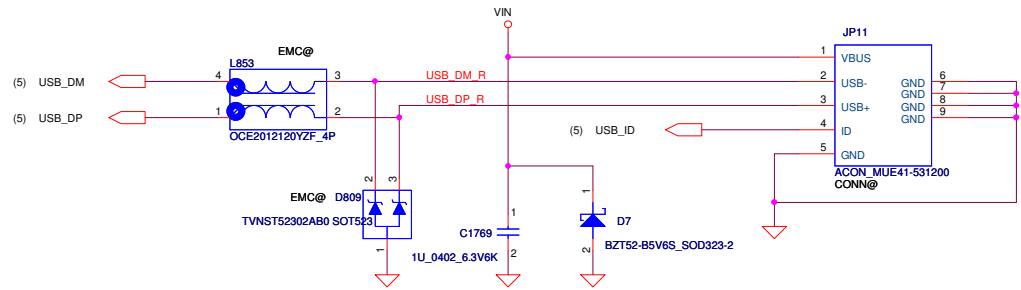


# Micro-USB

If mini-A connector insert => CID < 0V => Low  
 If mini-B connector insert => CID > 1.2V => High  
 IDPULLUP pin is replaced by 1.2V power source.

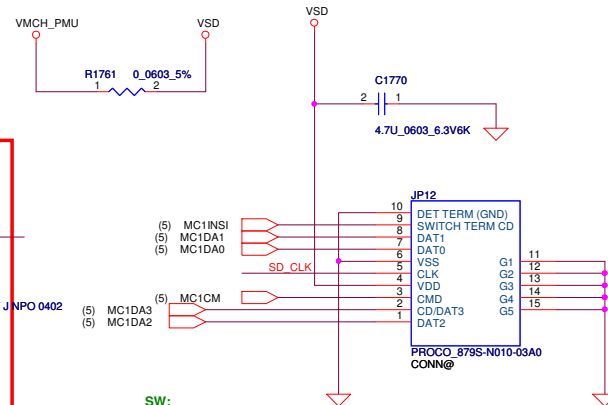
FOR RF request

TP1364PAD@ ← USB\_DM\_R  
 TP1365PAD@ ← USB\_DP\_R



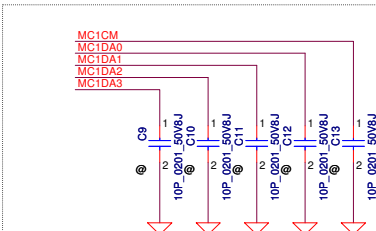
Compal GND      MTK GND

# SD card



EMI

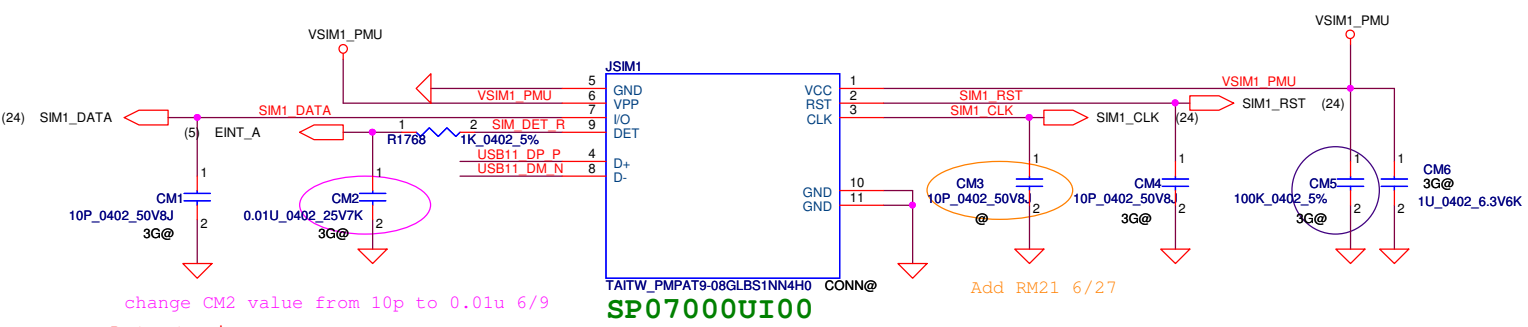
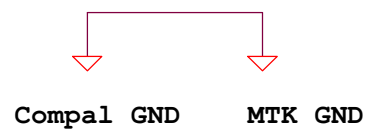
SW:  
 H: Card remove  
 L: Card insert



for RF request  
 close U201 side

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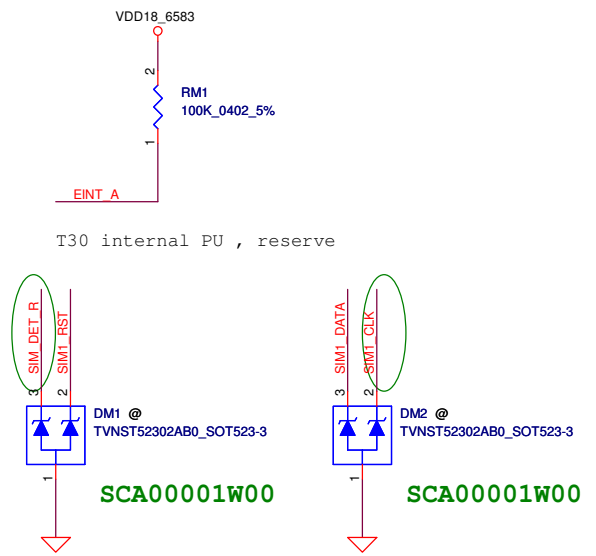
# SIM CARD



change CM2 value from 10p to 0.01u 6/9  
 Detect pin  
 Normal : short GND  
 Insert Card : Open

**SP07000U100**

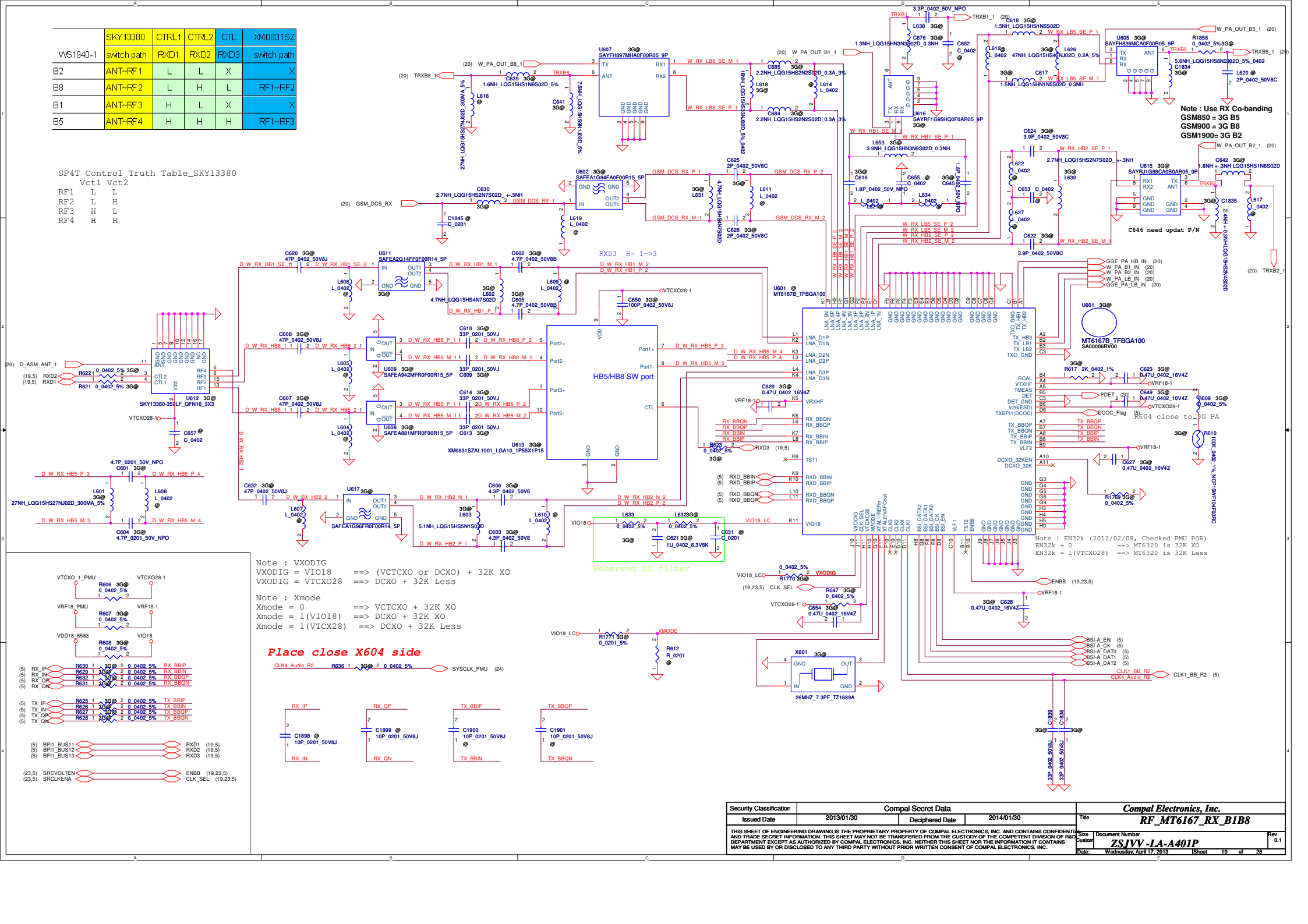
Change CM5 from 0.1uf to 100K for UIM discharge 7/24



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	SKY13380	CTRL1	CTRL2	CTL	XM0831SZ
WS1940-1	switch path	RXD1	RXD2	RXD3	switch path
B2	ANT-RF1	L	L	X	X
B8	ANT-RF2	L	H	L	RF1~RF2
B1	ANT-RF3	H	L	X	X
B5	ANT-RF4	H	H	H	RF1~RF3

SP4T Control Truth Table\_SKY13380  
 Vct1 Vct2  
 RF1 L L  
 RF2 L H  
 RF3 H L  
 RF4 H H

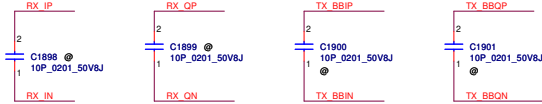


Note : VXODIG  
 VXODIG = VIO18 ==> (VTCXO or DCXO) + 32K XO  
 VXODIG = VTCXO28 ==> DCXO + 32K Less

Note : Xmode  
 Xmode = 0 ==> VTCXO + 32K XO  
 Xmode = 1(VIO18) ==> DCXO + 32K XO  
 Xmode = 1(VTCX28) ==> DCXO + 32K Less

Place close X604 side

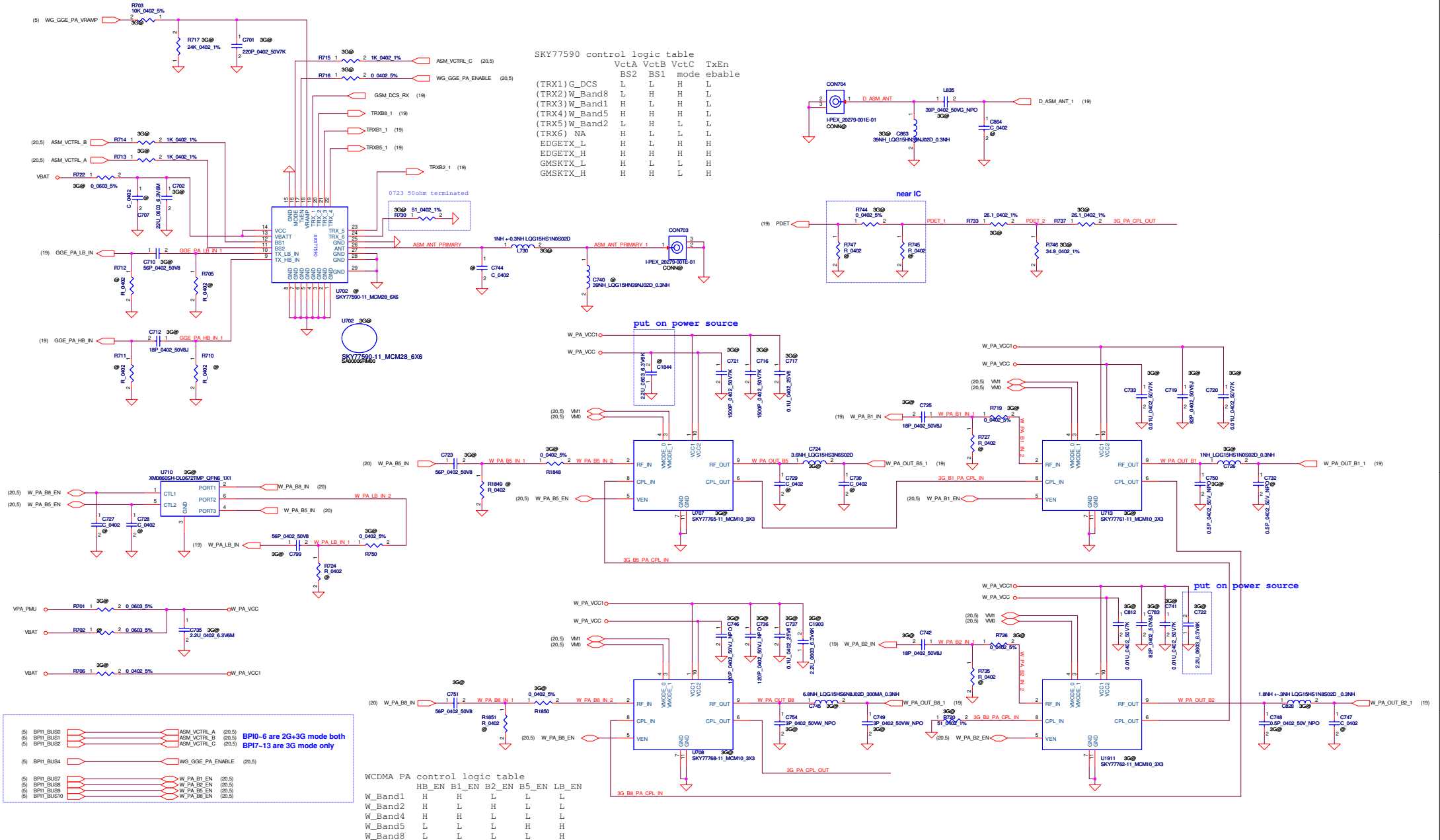
CLK4 Audio R2 R636 1 300 2 0.0402 5% SYSCLK\_PMU (24)

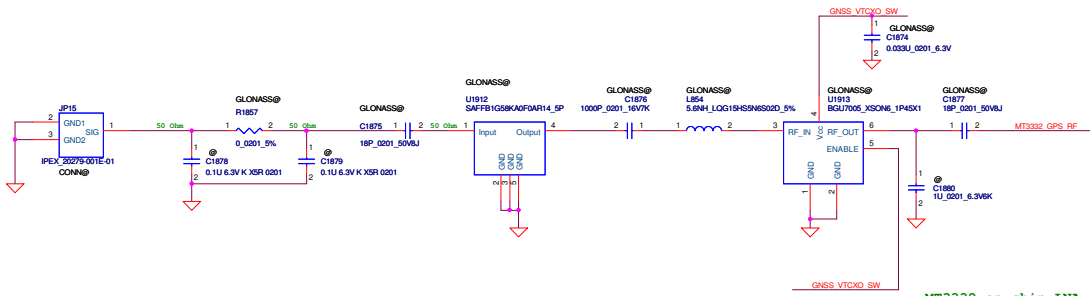


Reserved LC filter

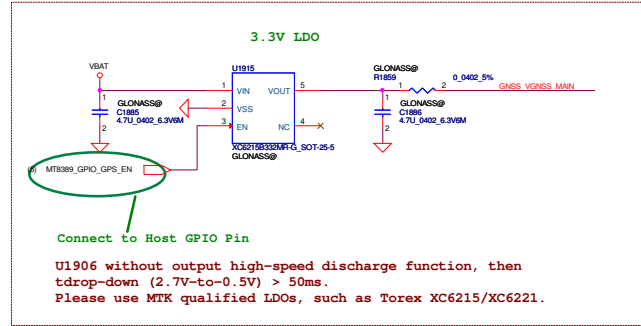
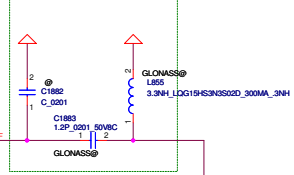
Note : Use RX Co-banding  
 GSM850 = 3G B5  
 GSM900 = 3G B8  
 GSM1900 = 3G B2

Security Classification	Compal Secret Data		Title	
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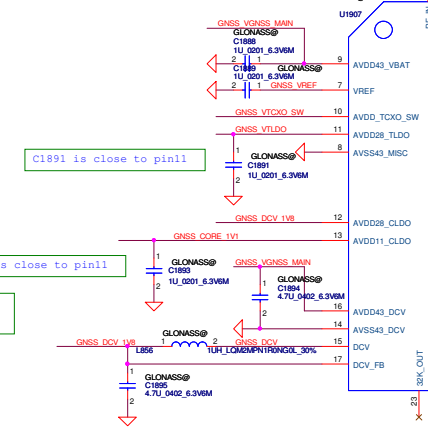
MT3332 on-chip LNA Matching



Connect to Host GPIO Pin  
 U1906 without output high-speed discharge function, then tdrop-down (2.7V-to-0.5V) > 50ms.  
 Please use MTK qualified LDOs, such as Torex XC6215/XC6221.

SA0006M400  
 S IC MT3332N QFN 48P GPS

# MT3332 QFN-48pins



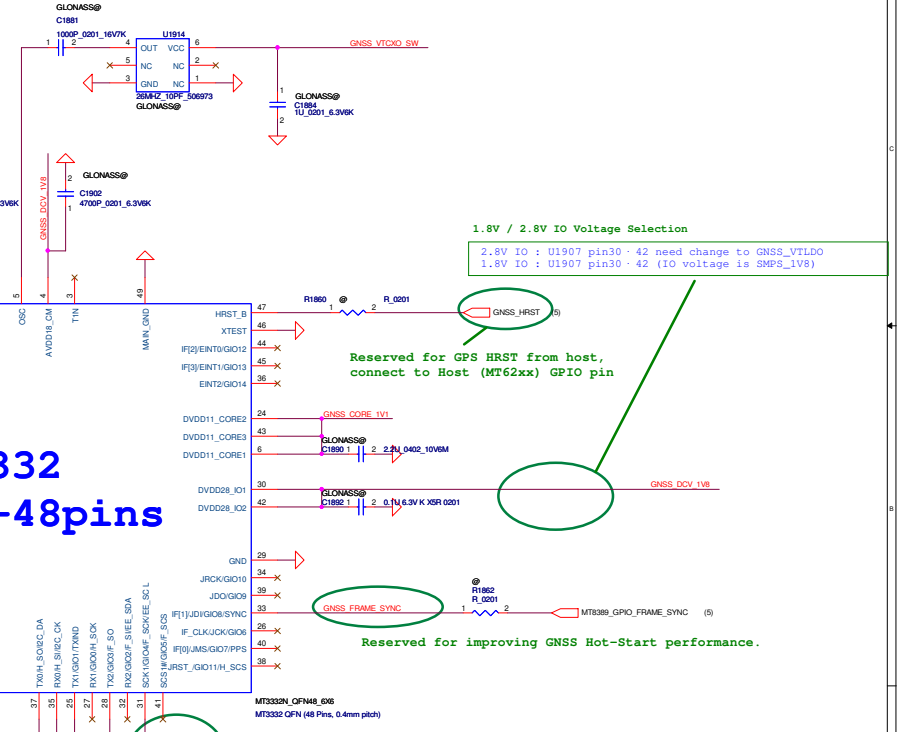
C1891 is close to pin11

C1893 is close to pin11

pin14 connect to C1894 GND net first, then connect to reference GND

RTC Voltage (2.8V)

Connect GNSS\_HOST\_VRTC to always alive voltage source, and keep the voltage swing of GNSS\_HOST\_32K RTC clock same as GNSS\_HOST\_VRTC.



1.8V / 2.8V IO Voltage Selection  
 2.8V IO : U1907 pin30 - 42 need change to GNSS\_VTLDO  
 1.8V IO : U1907 pin30 - 42 (IO voltage is SMPS\_IV8)

Reserved for GPS HRST from host, connect to Host (MT62xx) GPIO pin

Reserved for improving GNSS Hot-Start performance.

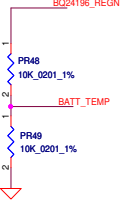
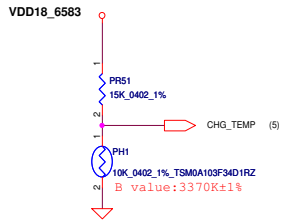
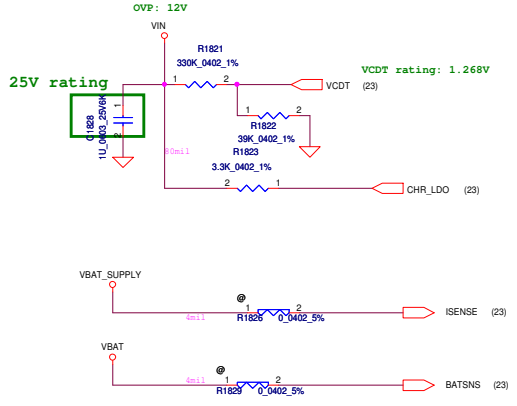
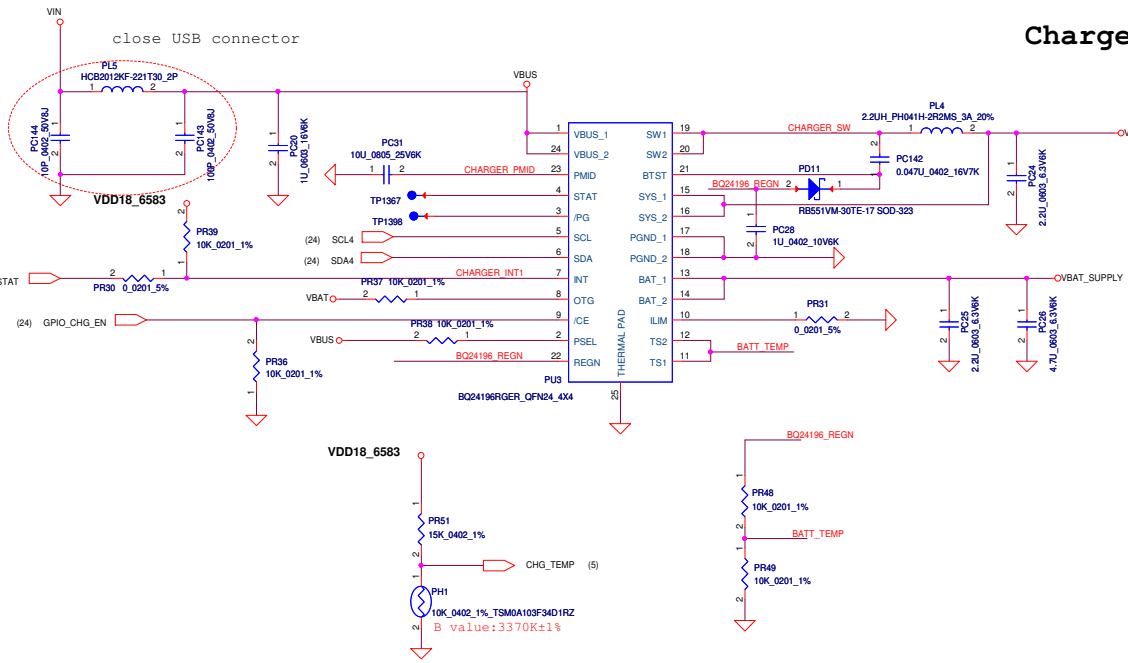
Reference Frequency Selection  
 16.368MHz TCXO : R1864 = NC, PIN\_41 = NC  
 26MHz TCXO : R1864 = 10K, PIN\_41 = NC  
 26MHz XTAL : R1864 = 10K, PIN\_41 contact 10K

As EINT to Host

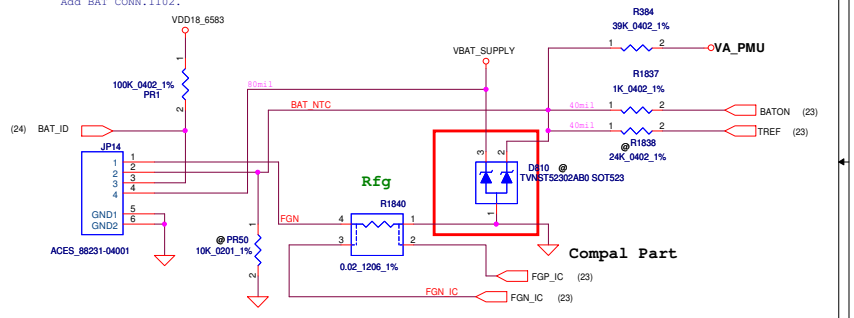
Connect to HOST UART (TX/RX) interface

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# Charger



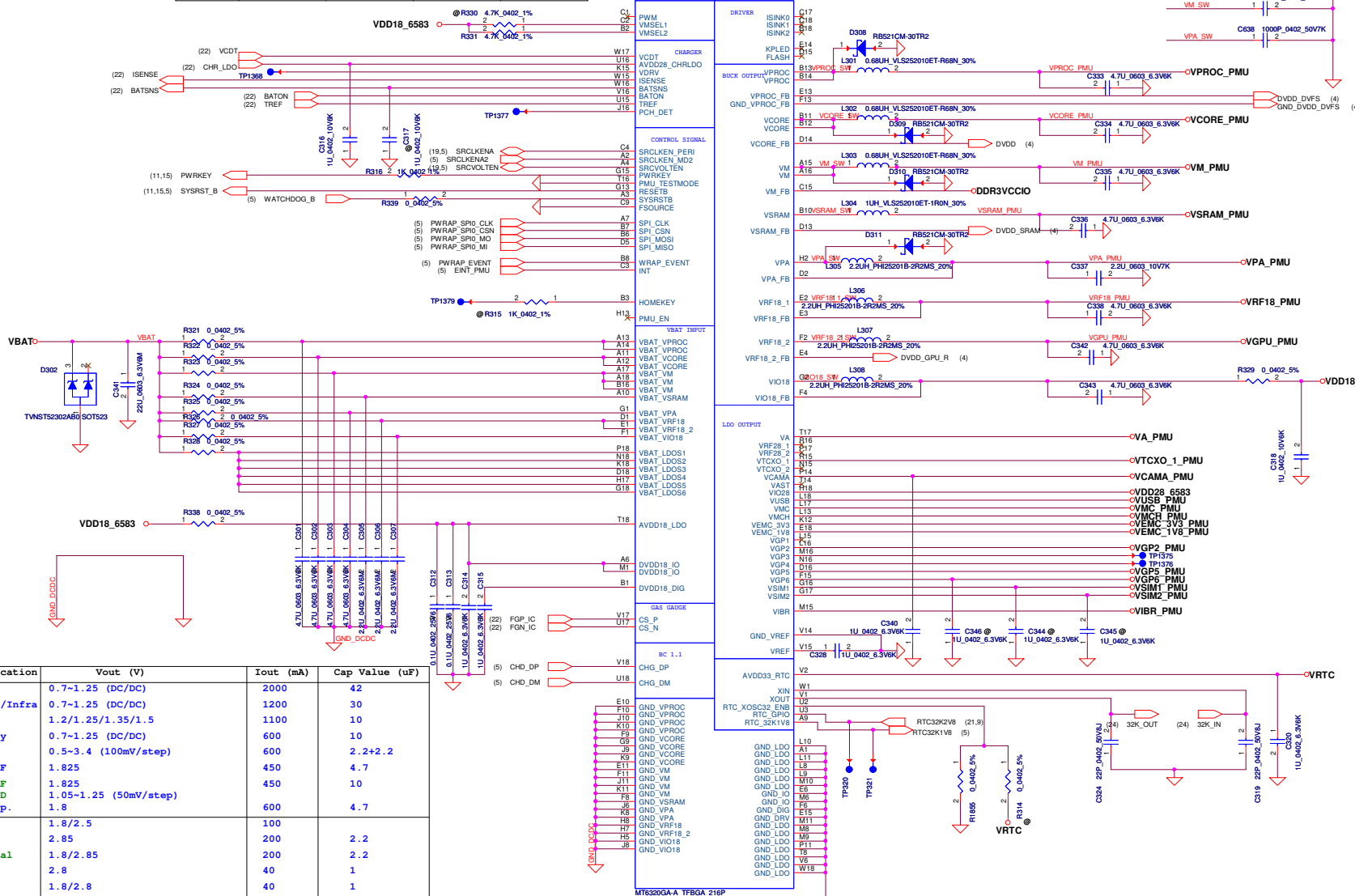
## BATTERY CONNECTOR



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PMIC

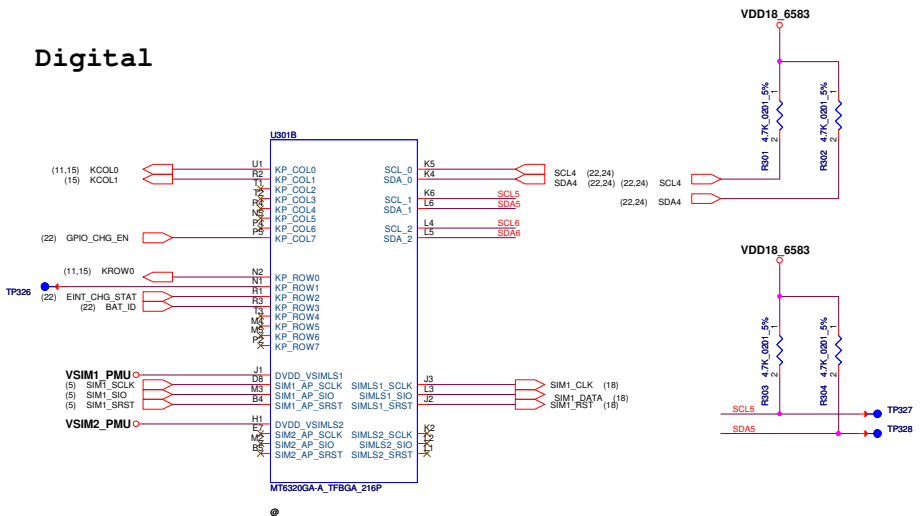
	LPDDR2/1.2V	DDR3U/1.25V	DDR3L/1.35V	DDR3/1.5V
VMSEL2	L	L	H	H
VMSEL1	L	H	L	H



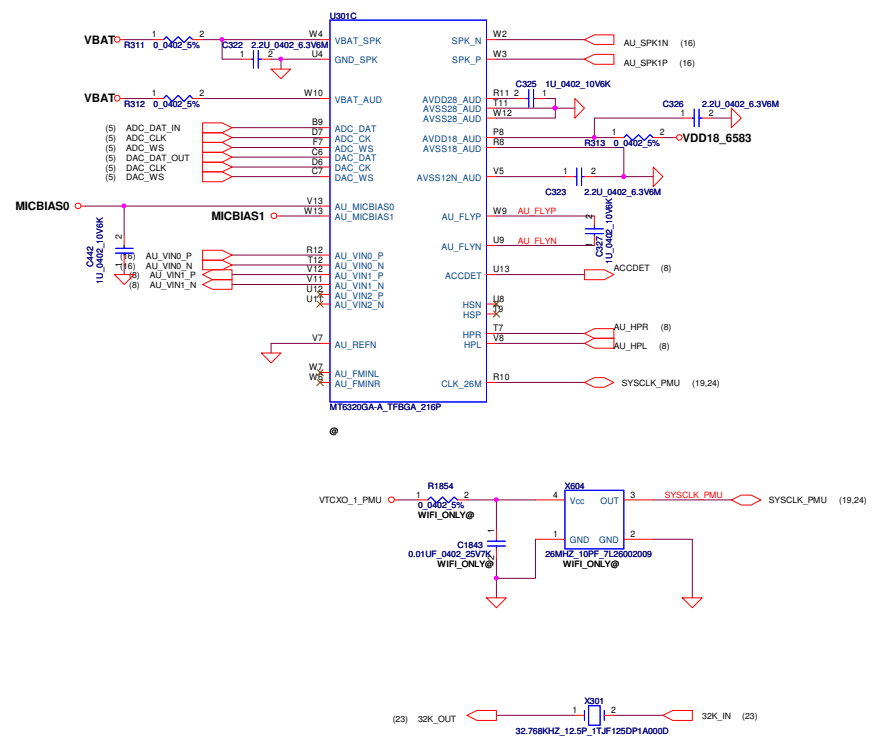
	Symbol	Application	Vout (V)	Iout (mA)	Cap Value (uF)
Buck	VPROC	CPU	0.7-1.25 (DC/DC)	2000	42
	VCORE	MDSYS/Infra	0.7-1.25 (DC/DC)	1200	30
	VM	VM	1.2/1.25/1.35/1.5	1100	10
	VDRAM	Memory	0.7-1.25 (DC/DC)	600	10
	VPA	3GPA	0.5-3.4 (100mV/step)	600	2.2+2.2
	VRF18_1	1st RF	1.825	450	4.7
	VRF18_2	2nd RF	1.825	450	10
Analog LDO	VIO18	GPU OD	1.05-1.25 (50mV/step)	600	4.7
	VA	MDSYS	1.8/2.5	100	2.2
	VRF28_1	General	2.85	200	2.2
	VRF28_2	General	1.8/2.85	200	2.2
	VTCXO_1	MDSYS	2.8	40	1
	VTCXO_2	MDSYS	1.8/2.8	40	1
	VCAMA	VCAMA	1.5/1.8/2.5/2.8	200	2.2
Digital LDO	VIO28	MT6168	2.8	400	2.2
	VAST	MT6168	0.9/1.0/1.1/1.2	300	2.2
	VUSB		3.3	200	1
	VMC	T-Card	1.8/3.3	200	1
	VMCH	T-Card	3.0/3.3	800	4.7
	VEMC_3V3	eMMC (Core)	3.0/3.3	800	4.7
	VEMC_1V8	eMMC	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	2.2
	VGP1	VCAMD	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	400	2.2
	VGP2	VCAM_IO	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VGP3	VCAM_AF	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VGP4	CTP/CMMB	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VGP5	CTP/CMMB	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VGP6	CTP/CMMB	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VSIM1	VSIM1	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
VSIM2	VSIM2	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1	
Vibrator	VTBR	Vibrator	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
RTC	VRTC	RTC Block	2.8	2	1-22

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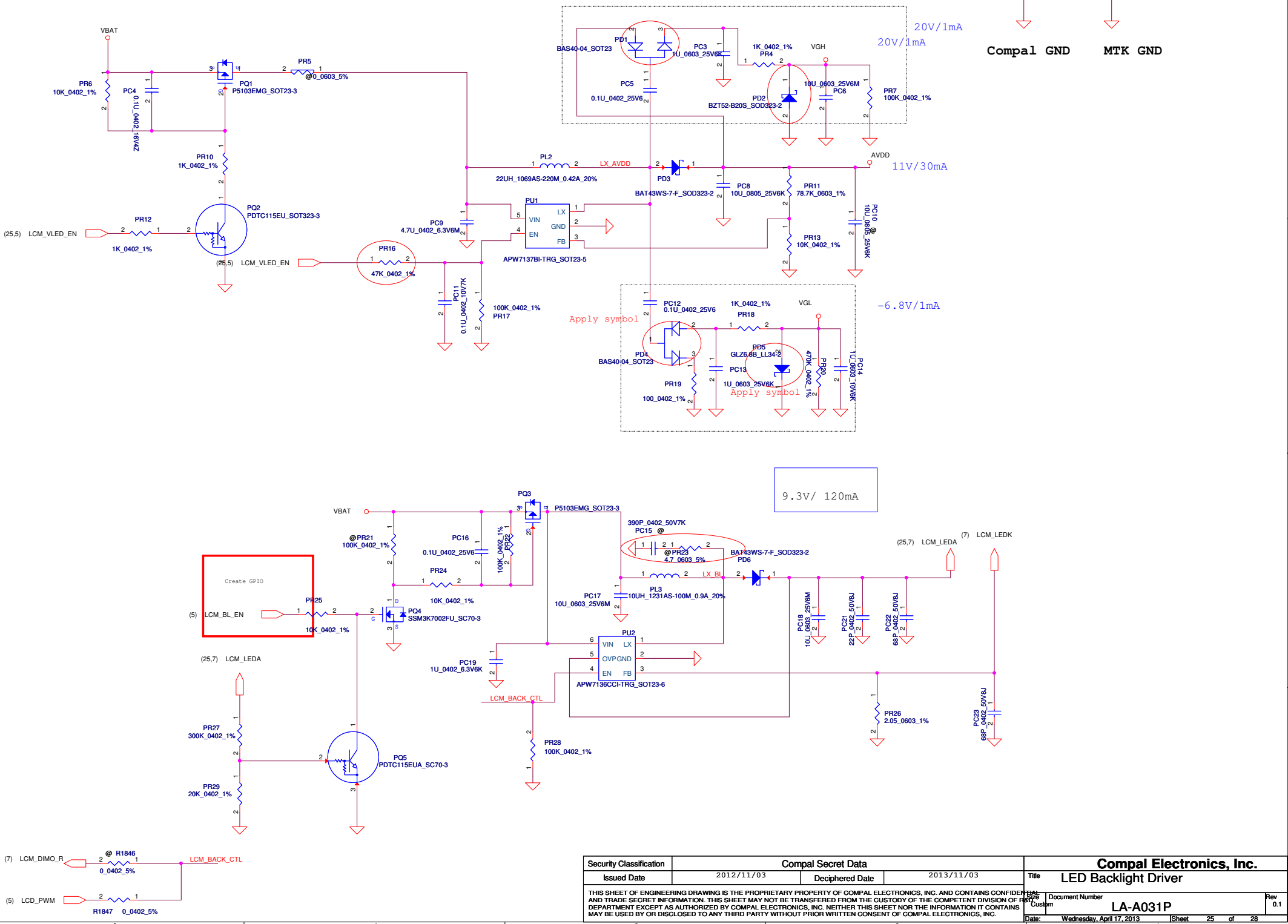
### Digital



### Audio







Compal GND MTK GND

20V/1mA  
20V/1mA

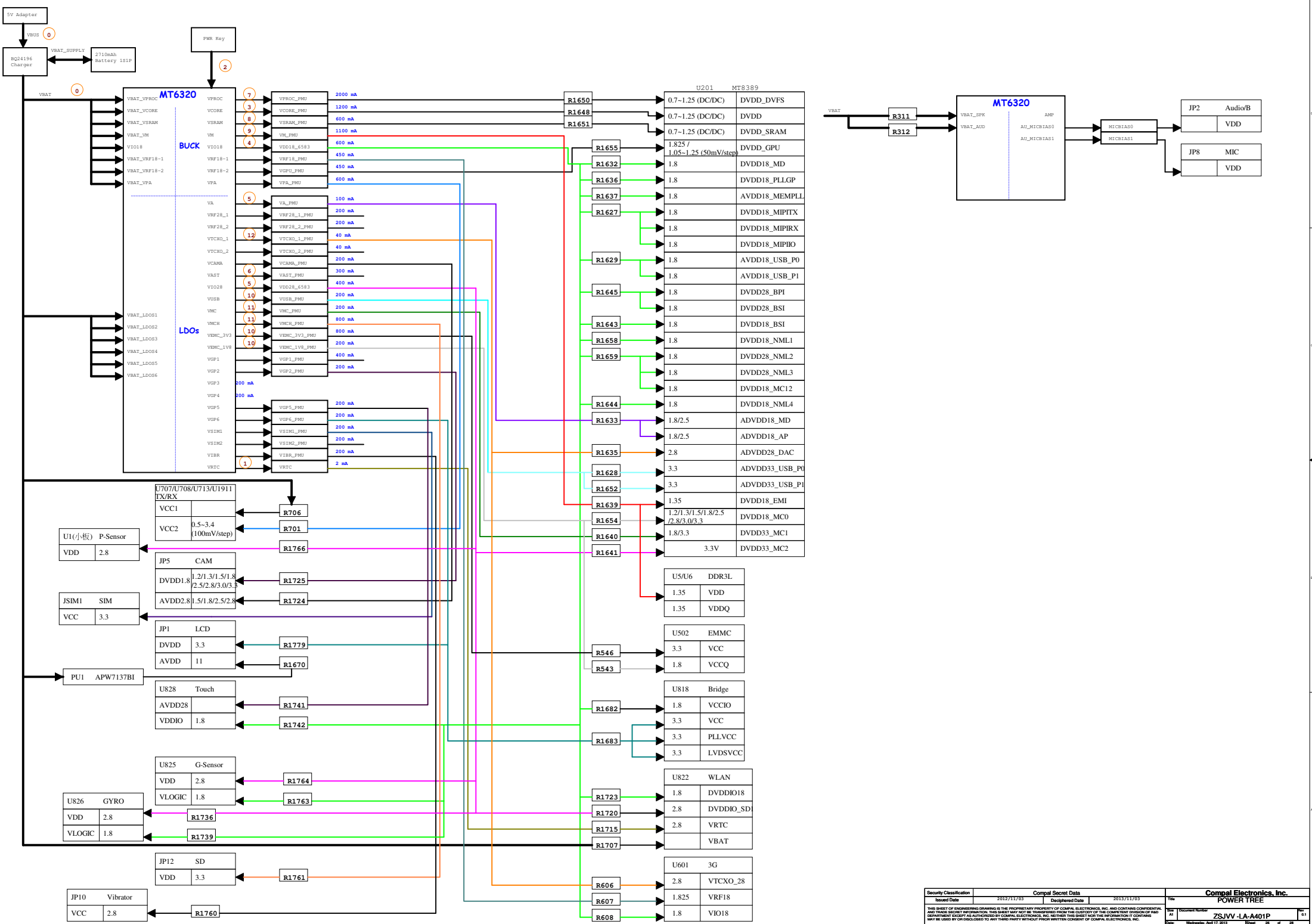
11V/30mA

-6.8V/1mA

9.3V/ 120mA

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<b>Compal Electronics, Inc.</b>	
<b>LED Backlight Driver</b>	
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2013/3/11  
 Update PD11 , D308 , D309 , D310 , D311 , L301 ,  
 L302 , L303 , L304 , L307 , C647 , C646 , C635 ,  
 C638 compal P/N  
 Change to un-pop : PR50 , R1838 , R314 ,R315  
 Change to pop : R1855

2013/3/13  
 Add C318

2013/3/14  
 Del R332,R348

2013/4/1  
 add R1847  
 reserve 0-ohm for panel design

2013/4/10  
 reserve C346 for VGP6 PMU  
 PR51 change to 15K\_0402\_1%  
 PH1 change to 10K\_0402\_1%

2013/4/15  
 Add PL5 , PC143 ,PC144 for EMI request  
 Add PC21 , PC22 ,PC23 for RF request

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2013/2/25  
P04. NC parts change to 0.luF\_0402\_NC  
R1648-R1651 to 0\_0603  
R1639 to 0\_0805  
P05. R634 from P19 to P05  
update X602 symbol  
del no Funcitn net :  
U201C\_AF10, U201D\_C29-J25, U201E\_G2  
P06. DEL TP1392PAD-TP1395PAD  
P07. DEL R1672,R1673,net cabc\_enable1/0  
C1687-C1689 change to 1U\_16V  
C1691-C1698 change to 0.1U\_10V%0.01U\_16V  
C1692,C1695 to @  
P08. DEL R1702,net ADC1\_ACCESSORY  
JP2\_PIN\_8 change to VEMC\_3V3\_PMU  
JP2\_PIN\_6 change to GND  
P09. R1711,R1716-R1719,R1721,R1722 to 0\_0201  
P11. DEL R1731,R1732, net UTXD1/URXD1\_DEBUG  
R1729,R1730 to short  
R1728,R1727 del @  
P12. R1764 to short  
U825 VDD28 6583 change to VDD18\_6583  
P13. DEL R1740, net VDD28\_6583  
H7 change to H\_1P5X2P0N  
P14. R1743,R1744 to short  
P15. SW3 PIN.3 to KCOL0  
SW4 PIN.3 to KCOL1  
P16. JP10 PIN.2 to GND  
P17. ADD D7  
ADD C9-C12 for RF request  
P18. DEL RM2  
R1765,R1766 move to U201 side  
Update 3G schematic:  
1.change size from 0402 to 0201 of R633,C631,R612,R1771  
2.Add shunt cap in RX matching circuit.  
3.Remove R645,U614,C644,R643  
Change C656,C643 bom structure to @  
4.remove R613  
5.change C610,C609,C614,C613 footprint from 0402 to 0201  
6. change C601,C604 footprint from 0402 to 0201  
(need update P/N)  
7 .Del R634 ( change to P5)

2013/2/26  
Update Block diagram,Notes list  
P05. DEL net URXD2,UTXD2,BF11\_BUSS5/6,VBIA5  
R1765 pin2 contact USB11\_DP\_P  
R1766 pin2 contact USB11\_DM\_N  
P06. C64 , C70 , C 68 change to 0201  
P08. JP2\_PIN2. del GND  
P09. Del net MT6620\_EEDI,MT6620\_SDI01  
RTCCLK\_6620,SYSRST\_B\_6620,PMU\_EN\_6620  
GPS\_SYNC\_6620  
P12. ADD R1764 for co-lay STK8313  
Update 3G schematic:  
1.Update C601,C604 P/N to SE000010K00  
2.C754,C749,C748,C750: @ to 3G@  
3.Change C733 to 0.01u  
4.add remind as below in C1844 and C722

2013/2/27  
P04. R1639 to 0805 short pad  
P05. R1765,R1766 change to 3G@  
P10. JF5 mirror horizontally  
P13. PAD1-3 change to S2-4  
P17. ADD C13  
C9-C12 change to @

2013/3/1  
P04. change R1639 footprint from 0805-s to 0805  
R1648,R1650 change to 0603 short pad  
update PWR schematic  
update 3G schematic  
Due to RX trace "交錯線"  
Change W\_RX\_HB1\_SE\_M\_1 to U616.8  
W\_RX\_HB1\_SE\_P\_1 to U616.1

2013/3/1 A  
P05. U201\_AH4,AF6 change to MB\_ID0/1  
U201\_AJ3,AH5,AG5 change to GPIO\_0-3  
ADD R1520-R1529,net CHG\_TEMP  
P11. DEL R1727  
update PWR schematic

2013/3/1\_B  
P04. R1648,R1650 change to 0805 short pad  
P21. update PU3 footprint  
P24. DEL PR3

2013/3/2  
update 3G schematic  
P19. U613.7 contact to D\_W\_RX\_HB5\_P\_3  
U613.8 contact to D\_W\_RX\_HB5\_M\_3  
update PWR schematic  
P22. GND\_DCCD contact to GND

2013/3/3  
update PWR schematic

2013/3/4  
P03. update MB\_ID table  
fix DRC error

2013/3/5  
update 3G schematic.  
Del TP1396,TP1397  
update PWR schemaitc  
fix DRC error

2013/3/6  
P05. net MB\_ID1 change to U201\_AA28  
net GPIO\_0 change to U201\_AA29

2013/3/7  
P07. ADD R1684 for IT6211VG  
ADD R1675,R1678, net CABE\_ENABLE0/1  
P09. U822\_PIN15 change to net MT6620\_1V8  
remove R1720, C1736  
Add P21. for GPS MT3332 circuit  
update 3G schematic  
P19. Add C1896-C1901  
del R633,R619,R620,R611

2013/3/8  
P13. DEL CLIP10,14, S4  
Update 3G schematic  
U601.A11 ----> NC

2013/3/8A  
P09. ADD R1713  
Update MT3332 schematic  
remove R1858,R1861,R1863,R1865  
R1866,R1868

2013/3/9a  
Update 3G schematic  
modify C1898,C1899 net name

2013/3/11  
Add P26 POWER\_PIR  
P21. Update L856 LIB & P/N  
update PWR schematic

2013/3/12  
update block diagram  
add power tree page

2013/3/13  
ADD NH520@,NH520\_EMC@  
modify RAM BOM structure  
P01 Add S4 for GLONASS frame  
P05. Del TP1373  
P07 R1675,R1678 to @  
ADD C1772,C1773 for RF request  
P09. update U823 symbol  
P13. R535 to 27ohm(MTK advice)  
P15. R1753,C1759 to @ (MTK advice)  
P17. ADD TP1364,TP1365 for RF request  
update 3G schematic  
delete C643,C656,TP601,TP602

2013/3/14  
P05. ADD TP1366,TP1369  
P21. C1887,C1902-->SE00000WN00  
C1888,C1889,C1891,C1893-->SE00000UC00  
C1890-->SE00000V600  
update 3G schematic  
Add C1903 for U708.

2013/3/18  
L838,L839,L840,L841,L842,L853  
change to SM070001R00

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